

200W, HF-0.5GHz 50V High Power RF LDMOS

Description

The MV0520VX is a 200W single ended 50V LDMOS, unmatched for any applications within HF-0.5GHz

At 28V, it also works as 100W single ended LDMOS as the drop-in replacement of legacy VDMOS like BLF246/MRF174/DU2880U in the same mechanical outlines while with improved performance and ruggedness

It supports CW, and pulsed and any modulated signal at either saturated or linear application.



- Typical performance(on Innogration test board with device soldered)

Signal: CW,

Freq(MHz)	Vds(V)	Pin(dBm)	Pout(W)	Gain(dB)	Eff(%)
108	50	33	200	20	70
108	28	33	100	17	70

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^{\circ}\text{C}$, $T_J=200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.60	°C/W

MV0520VX LDMOS TRANSISTOR

Document Number: MV0520VX
Preliminary Datasheet V1.1

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

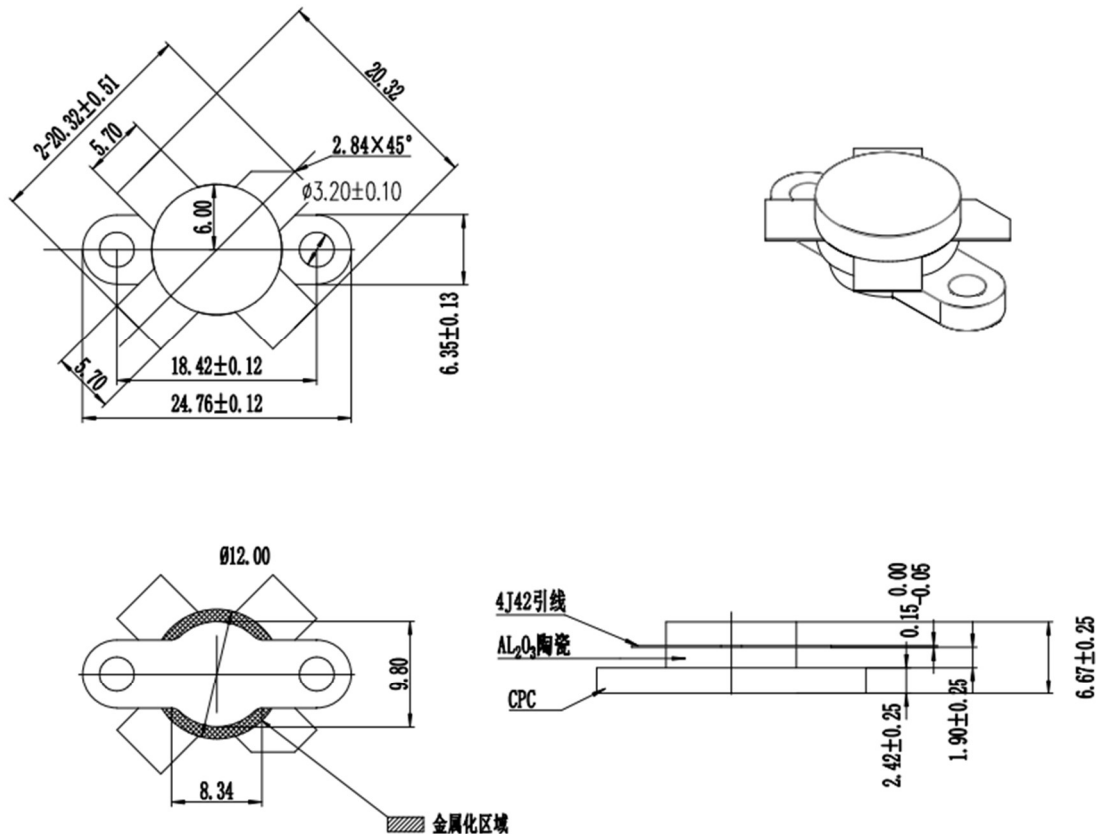
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}, V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}, I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}, I_D = 100\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.1	—	V
Drain source on state resistance ($V_{DS}=0.1\text{V}, V_{GS}=10\text{V}$)	$R_{ds(on)}$		217		$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{ISS}		158		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{OSS}		46.8		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{RSS}		1.24		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 100\text{mA}$, $f = 160\text{MHz}$, pulse width: 100us, duty cycle: 10%

Load 20:1 All phase angles, at 050W Pulsed CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate、2—Drain、3—Source)



技术要求:

1. 未注尺寸公差±0.15;
2. 全镀金: 外底面、内腔以及引线中心Ni: 2.54-11.43 μm, 金2.54-4 μm;
3. 图示阴影部分为金属化区。
4. 单位:mm.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/3/26	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing

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