

MV0517VX LDMOS TRANSISTOR

Document Number: MV0517VX
Preliminary Datasheet V2.0

170W, HF-0.5GHz 50V High Power RF LDMOS

Description

The MV0517VX is a 170W single ended 50V LDMOS, unmatched for any applications within HF-0.5GHz

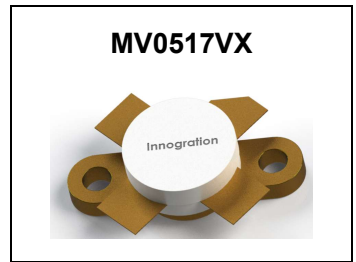
At 28V, it also works as 80W single ended LDMOS as the drop-in replacement of legacy VDMOS like MRF173 in the same mechanical outlines while with improved performance and ruggedness

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

- Typical performance(on Innogration test board with device soldered)

Signal: CW , Vgs=3.4v, Vds=50v, Idq=180mA

Freq (MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	IDS (A)	Gain (dB)	Eff (%)	2 nd harmonic (dBc)	3 rd harmonic (dBc)
123	27.8	52.15	164.1	4.22	24.35	78	-26	-35
128	27.7	51.99	158.1	3.98	24.29	79	-26	-36
133	28.6	51.47	140.3	3.53	22.87	79	-26	-37



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+125	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.8	°C/W

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}, V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}, I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}, I_D = 180\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.4	—	V
Drain source on state resistance ($V_{DS}=0.1\text{V}, V_{GS}=10\text{V}$)	$R_{ds(on)}$				$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{ISS}				pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{OSS}				pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$)	C_{RSS}				pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 100\text{mA}$, $f = 160\text{MHz}$, pulse width:100us, duty cycle:10%

Load 20:1 All phase angles, at 250W Pulsed CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 128MHz

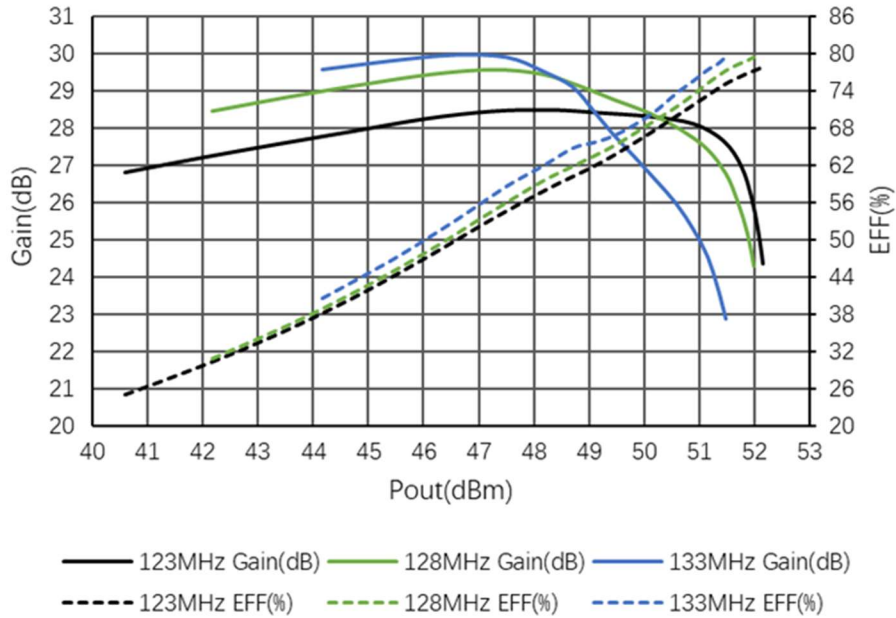
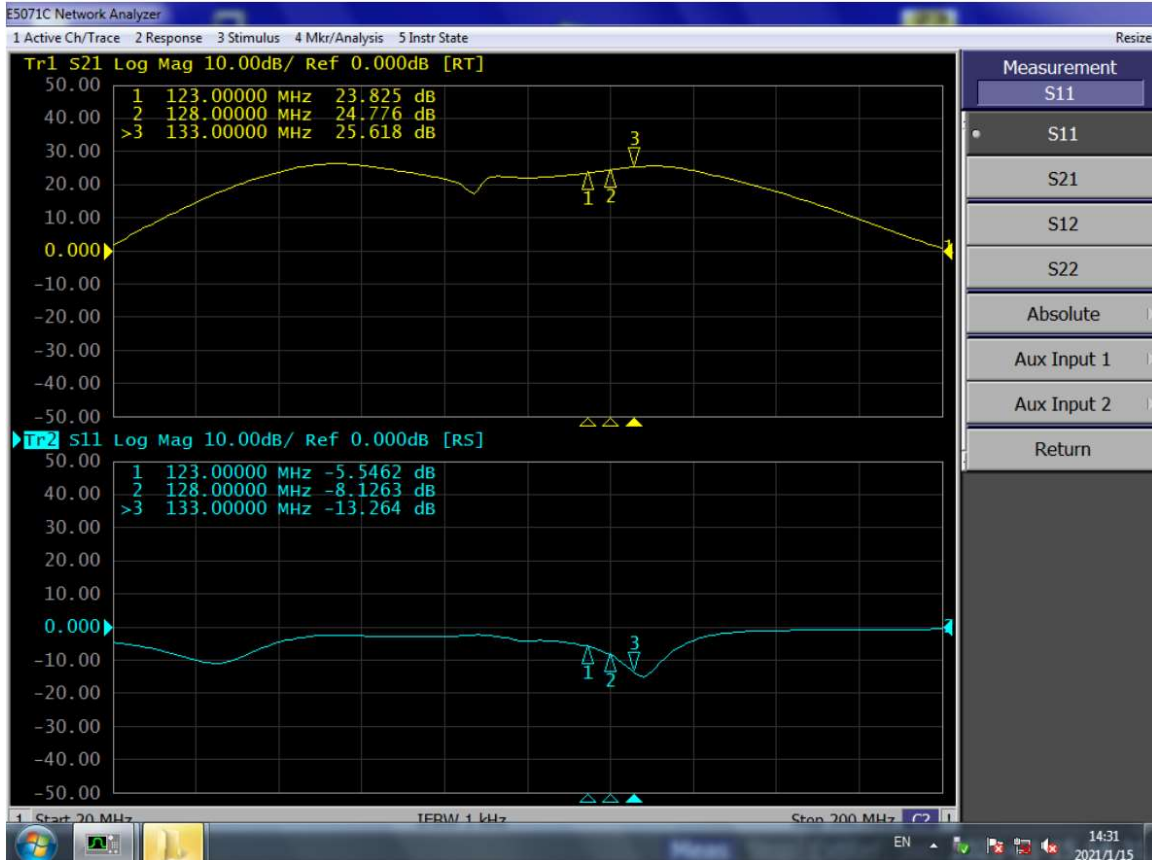
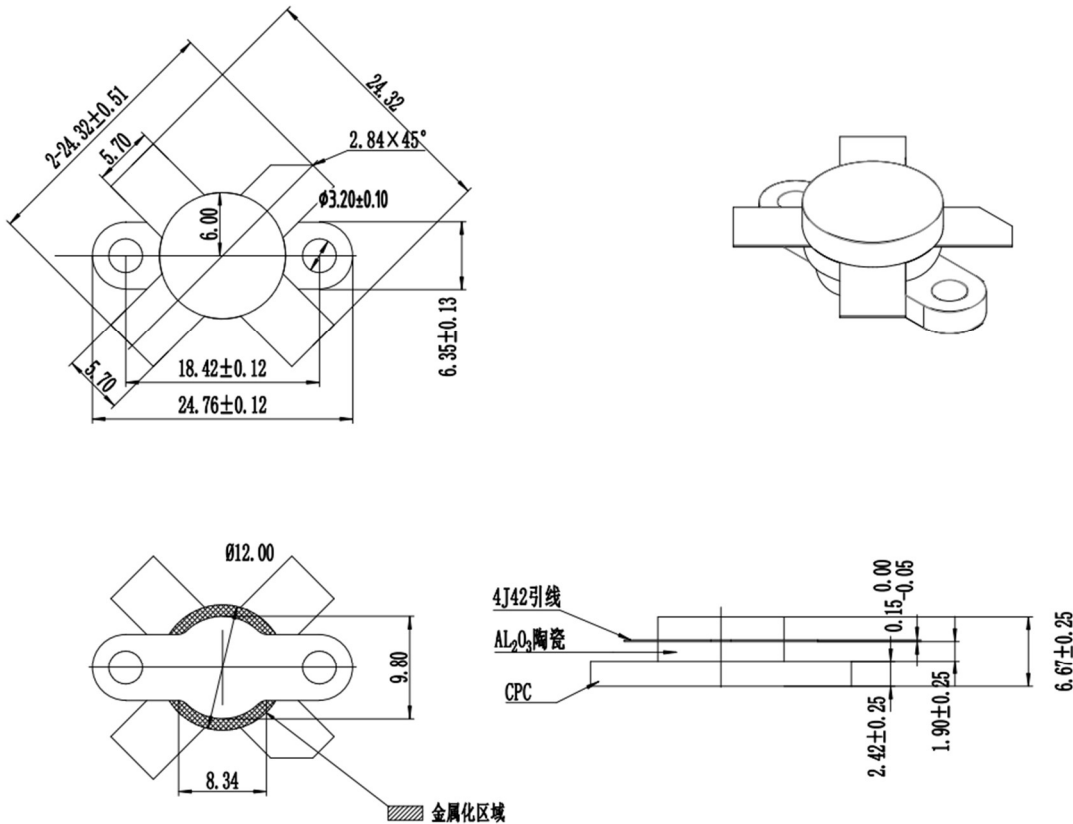


Figure 1: Network analyzer output S11/221



Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate、2—Drain、3—Source)



技术要求:

1. 未注尺寸公差±0.15;
2. 全镀金: 外底面、内腔以及引线中心Ni:2.54-11.43 μm, 金2.54-4 μm;
3. 图示阴影部分为金属化区。
4. 单位:mm.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/6/22	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing
2023/11/21	Rev 2.0	Modify drawing of extended leads length

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