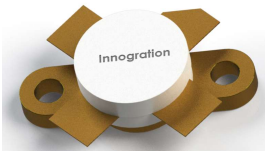
MV1503V LDMOS TRANSISTOR

Document Number: MV1503V
Preliminary Datasheet V2.0

30W, HF-1.5GHz 50V High Power RF LDMOS

MV1503V



Description

The MV1503V is a 30W single ended 50V LDMOS, unmatched for any applications within HF-1.5GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It can be the drop-in replacement of its equivalent 30W single ended VDMOS like MRF148A with higher efficiency, improved thermal performance and stability,

- Typical Performance (On Innogration narrow band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 100 mA, CW.

Frequency	Gp (dB)	P_{out} (W)	η_D@P_{out} (%)
162.5MHz	28	39	70

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	120	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.95	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

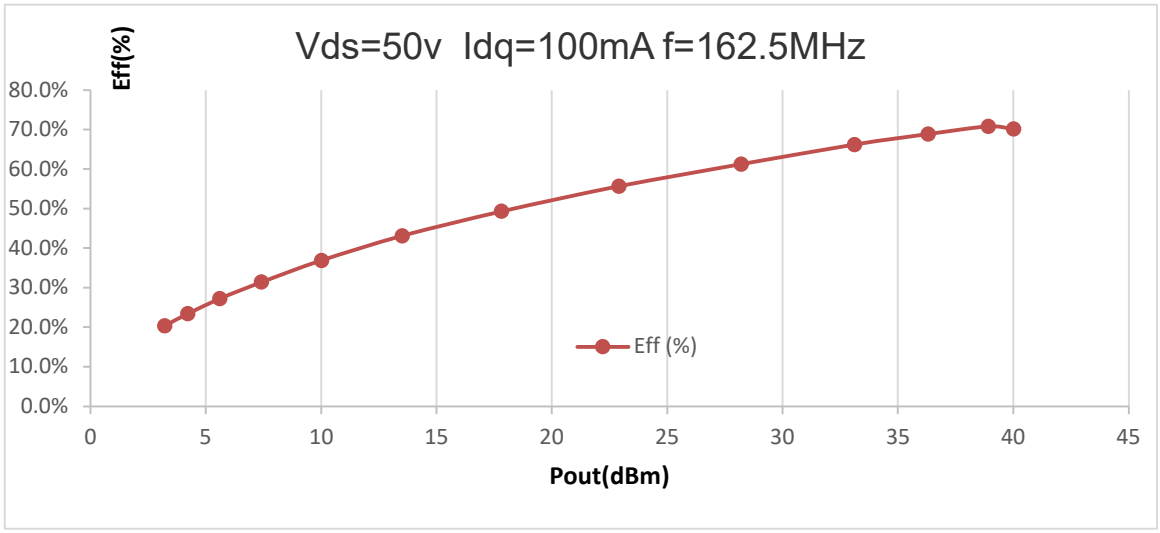
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

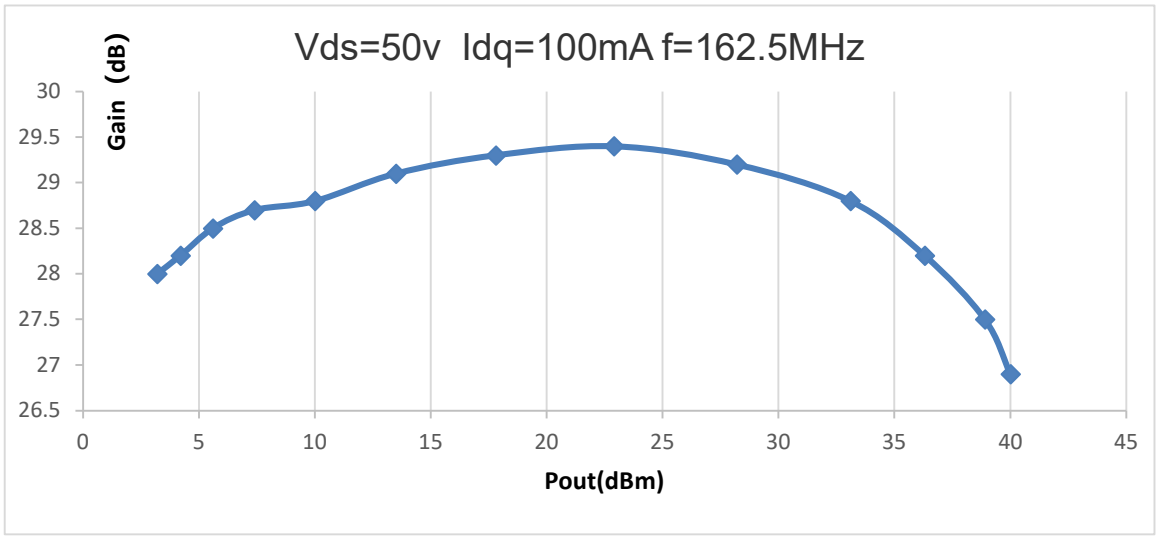
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		120		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.57	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		28.3		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		11.9		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.38		pF
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100mA, f = 915 MHz, CW Signal Measurements, Pin=21.5dBm					
Power Gain@Pout	G_p	——	24	——	dB
Output Power	Pout	30	36		W
Drain Efficiency@Pout	η_D	——	60	——	%
Input Return Loss	IRL	——	-7	——	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 162.5MHz

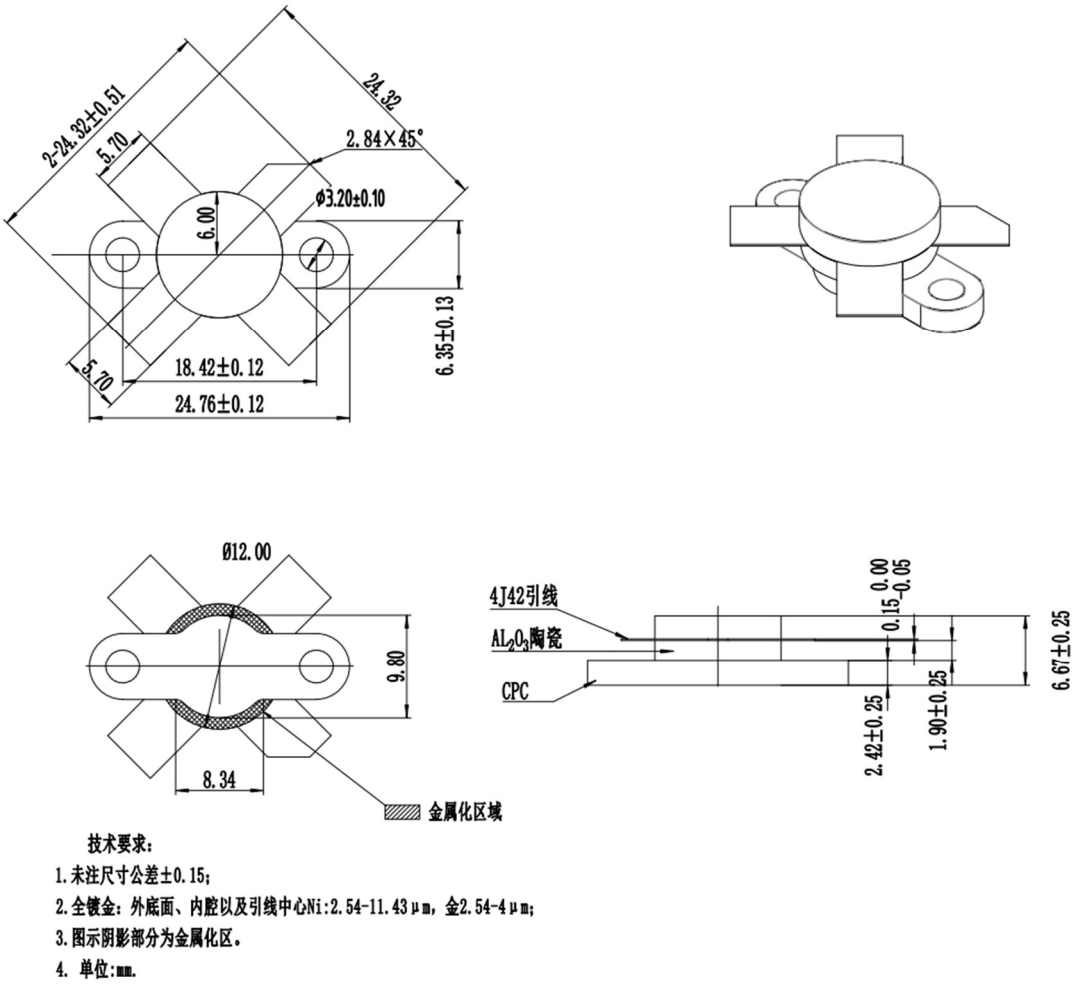
Signal：CW Vgs=3.72V, Vds=50V, Idq=100mA





Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—Gate、2—Drain、3—Source）



技术要求：

1. 未注尺寸公差±0.15；
2. 全镀金：外底面、内腔以及引线中心Ni:2.54-11.43μm，金2.54-4μm；
3. 图示阴影部分为金属化区。
4. 单位:mm.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/6/24	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing
2023/11/21	Rev 2.0	Modify drawing of extended leads length

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