

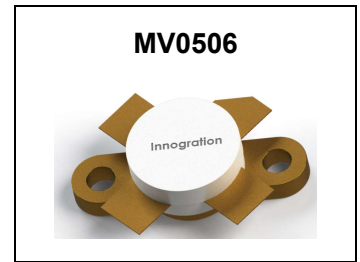
60W, HF-1GHz 28V High Power RF LDMOS

Description

The MV0506 is a 60W single ended 28V LDMOS, unmatched for any applications within HF-1GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It is also intended to be the drop-in replacement of legacy VDMOS such as MRF171A etc in the same mechanical outline while with improved performance



•Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 50$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D@P_{-1}$ (%)
1000 MHz	19	60	60

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_j = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

MV0506 LDMOS TRANSISTOR

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Preliminary Datasheet V2.0

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}	95	—		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{loss}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{loss}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{gss}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 400 μA)	V _{GS(th)}	—	2.2	—	V
Gate Quiescent Voltage (V _{DD} = 28 V, I _D = 50 mA, Measured in Functional Test)	V _{GS(Q)}	—	2.9	—	V
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{ISS}		69.2		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{OSS}		28.6		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{RSS}		1.1		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 50mA, f = 1000 MHz, CW Signal Measurements.

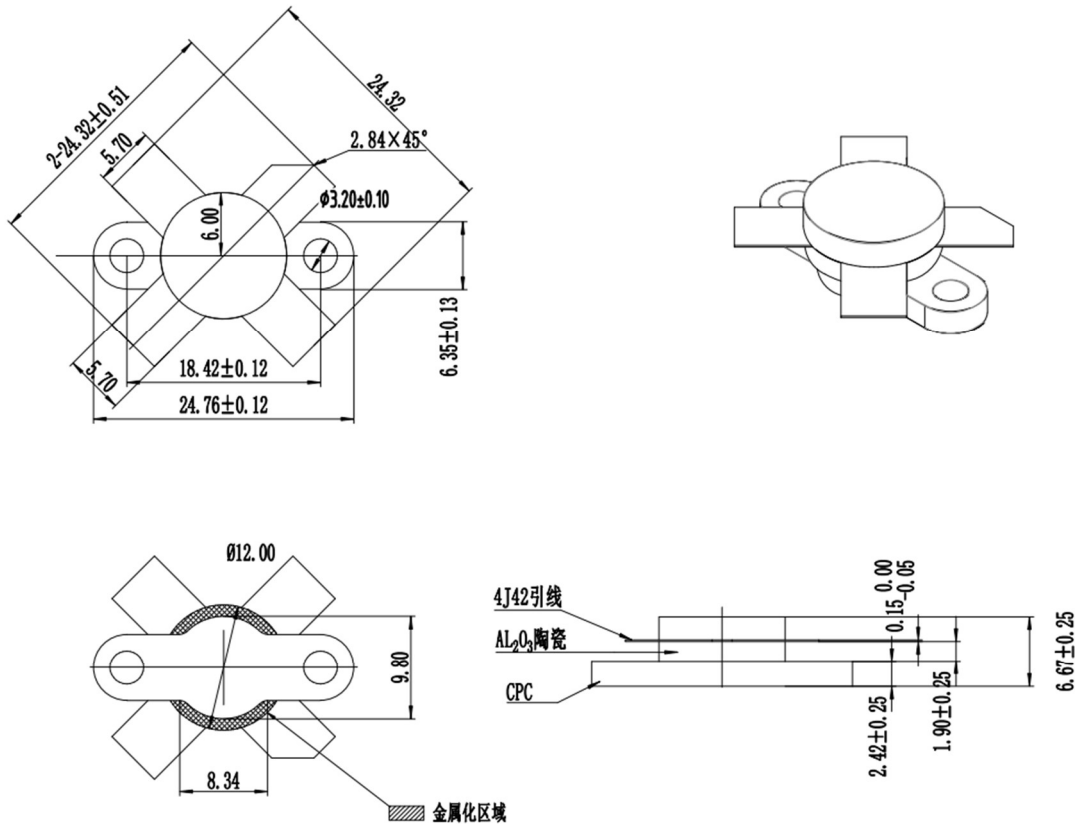
Power Gain	G _p	—	19	—	dB
Drain Efficiency@P1dB	η _p	—	60	—	%
1 dB Compression Point	P _{-1dB}	—	60	—	W
Input Return Loss	IRL	—	-7	—	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 350 mA, f = 1000 MHz

VSWR 20:1 at 60W pulse CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate、2—Drain、3—Source)



技术要求:

1. 未注尺寸公差±0.15;
2. 全镀金: 外底面、内腔以及引线中心Ni:2.54-11.43 μm, 金2.54-4 μm;
3. 图示阴影部分为金属化区。
4. 单位:mm.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/3/26	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing
2023/6/17	Rev 1.2	Add number indication of Pins on page 3
2023/11/21	Rev 2.0	Modify drawing of extended leads length

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