

SU2024V GaN TRANSISTOR

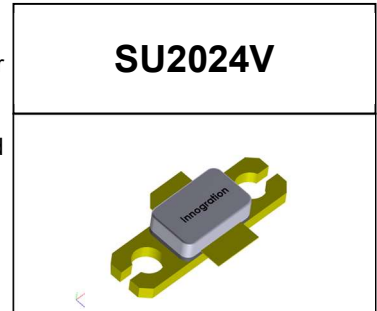
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Preliminary Datasheet V1.0

Gallium Nitride 50V 240W, RF Power Transistor

Description

The SU2024V is a 240W single ended, internally prematched GaN HEMT, designed for multiple applications with frequencies up to 2GHz.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.



- Typical performance (on fixture with device soldered): $V_{DD}=50V$ $I_{DQ}=200mA$, Pulse CW, Pulse Width=20 us, Duty cycle=10% $P_{sat}=P_{3dB}$

Freq(MHz)	P1dB(dBm)	P1dB(W)	P1dB Eff(%)	P1dB Gain(dB)	Psat(W)	Psat Eff(%)
1400	54.01	251.9	54.4	16.87	302.6	58
1500	53.63	230.7	55.3	17.7	308.4	60
1600	53.25	211.5	56.2	17.69	301.0	62
1700	53.00	199.5	57.7	17.3	299.7	66
1800	52.52	178.7	57.6	17.27	272.8	67

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	I_{gf}	30.2	mA
Storage Temperature Range	T_{stg}	-65 to +150	C
Case Operating Temperature	T_c	-55 to +150	C
Operating Junction Temperature	T_j	+225	C

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC Power Dissipation, FEA	$R_{\theta JC}$	0.8	C/W

Table 3. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 30.2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 50\text{V}$, $I_D = 30.2\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 200\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 200\text{mA}$, $f = 1600\text{MHz}$, Pulsed CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P3dB	Gp		14		dB
Drain Efficiency@P3dB _t	Eff		65		%
3dB Compressed point	P3dB	240	270		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		Ψ

Reference Circuit of Test Fixture Assembly Diagram

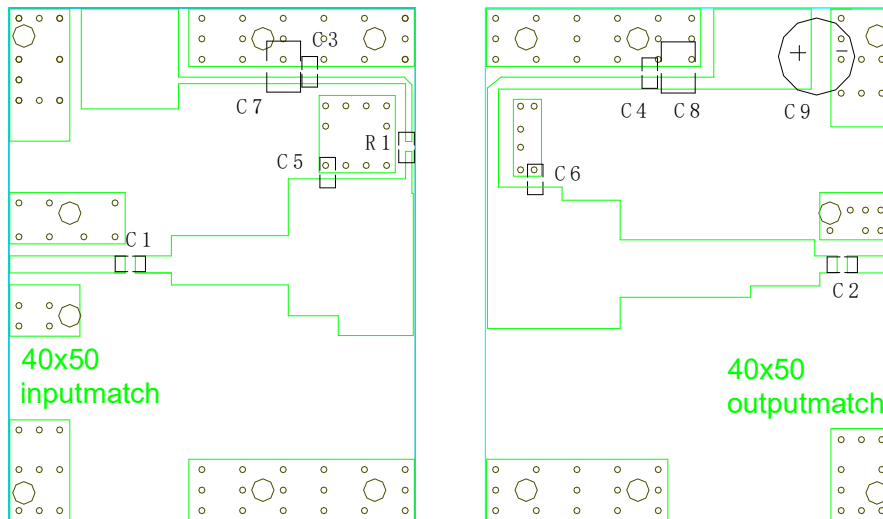


Figure 1. Test Circuit Component Layout (1400MHz~1800MHz)

Table 4. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1, C2, C3, C4	27pF	0805	4
C5	2.0pF	0805	1
C6	1.0pF	0805	1
C7, C8	10uF/100V	1210	2
C9	1000uF/63V		1
R1	10ohm	0603	1
PCB	RO4350B 30mils		1

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Figure 2. Pulse CW RF performance (1400MHz~1800MHz)

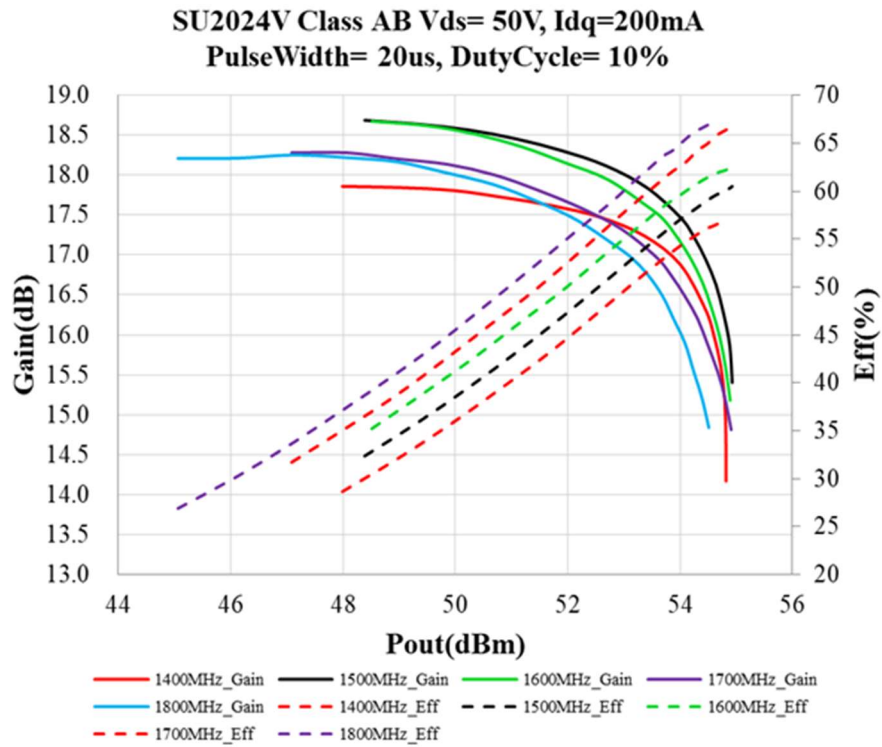
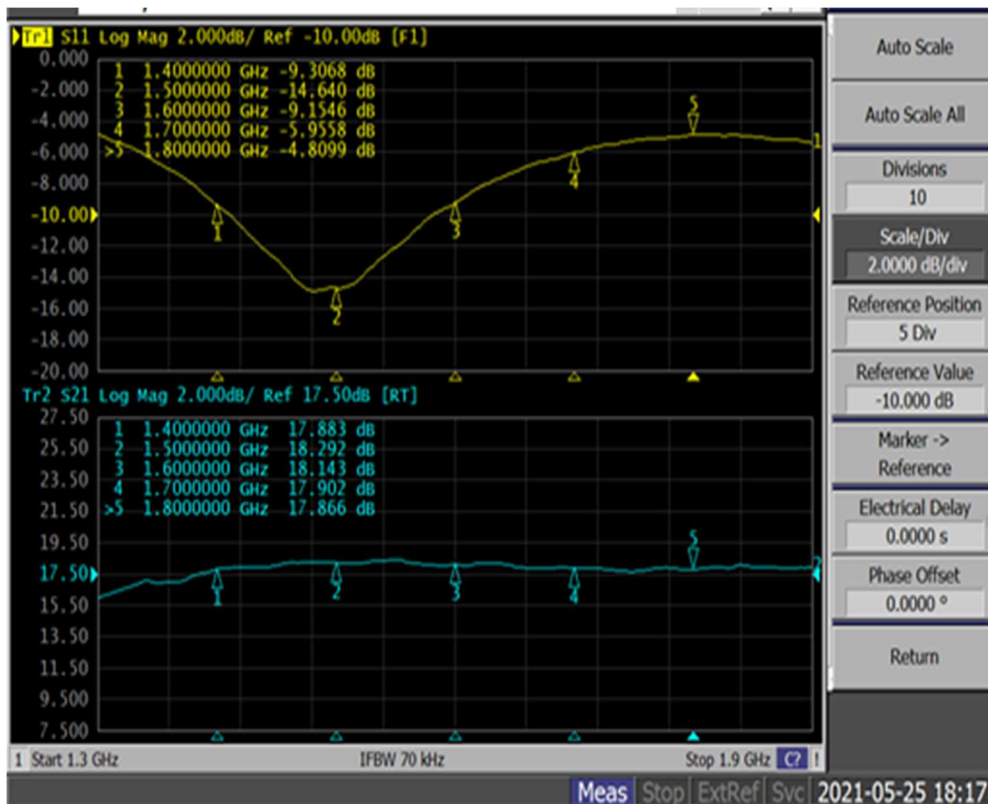


Figure 3. Network Analyzer result S11 and S21 (1100MHz~1500MHz) $V_{gs} = -3.0V$, $V_{DS}= 50V$, $I_{DQ} = 200mA$



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Package Outline

Flanged ceramic package; 2 leads

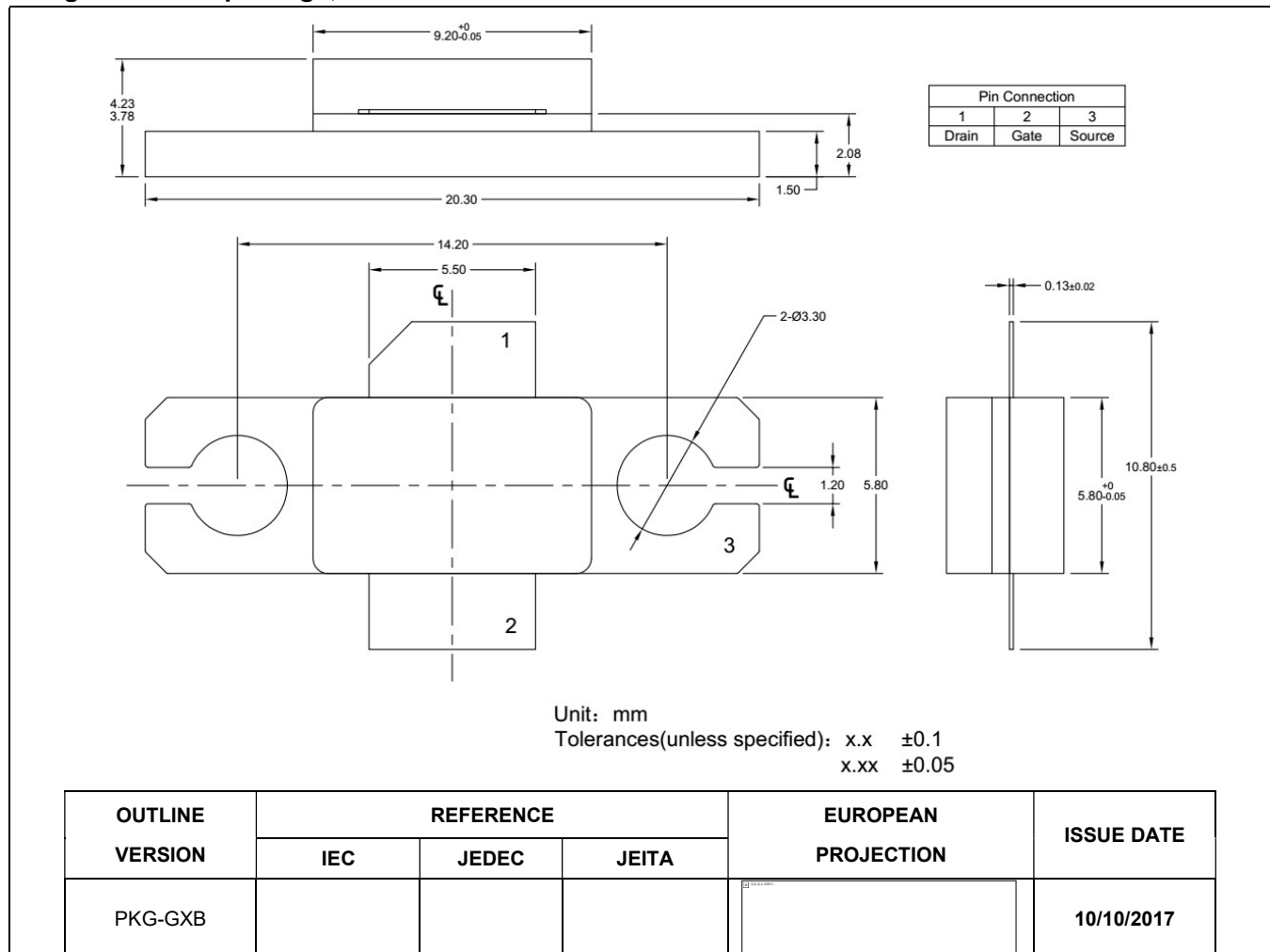


Figure 1. Package Outline PKG-G2E

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Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/7/12	V1.0	Modify the part number from SU3024V to SU2024V

Application data based LSM-21-11

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