Gallium Nitride 50V, 60W,4.8-5GHz RF Power Transistor

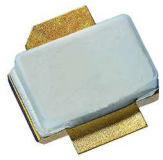
Description

The STAV50061G2 is a single ended 60watt, GaN HEMT, ideal for 5G NR applications from 4.8-5GHz.

It is an internally matched transistor capable of supporting CW, pulse or any modulated signal.

There is no guarantee of performance when this part is used outside of stated frequencies.

STAV50061G2



- Typical pulse CW performance across **4.8-4.9GHz**

V_{DD} = 48 Vdc, I_{DQ} = 80mA, Pulse width=20us, duty cycle=10%, Tc=25°C

(On innogration application board with device soldered)

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)	P4dB (dBm)	P4dB (W)	P4dB Eff(%)
4800	46.63	46.1	57.2	14.58	48.16	65.5	64.0	48.35	68.4	64.7
4850	46.62	45.9	57.3	14.48	48.2	66.1	63.9	48.39	69.0	64.4
4900	46.58	45.5	55.7	14.43	48.17	65.7	61.9	48.38	68.8	62.6

Applications

- Sub-4GHz pulse or CW amplifier
- 5G Class AB or Doherty power amplifier
- Wideband jammer

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

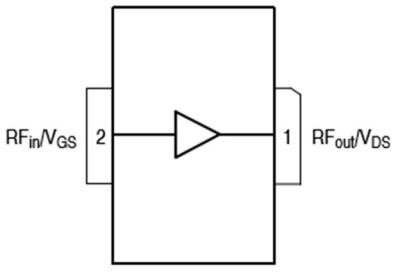


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	8	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=40W Pulsed CW	$R_{\theta JC}$	TBD	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=8mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 8mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=80mA, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	4.9GHz, Pout=60W pulse CW All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

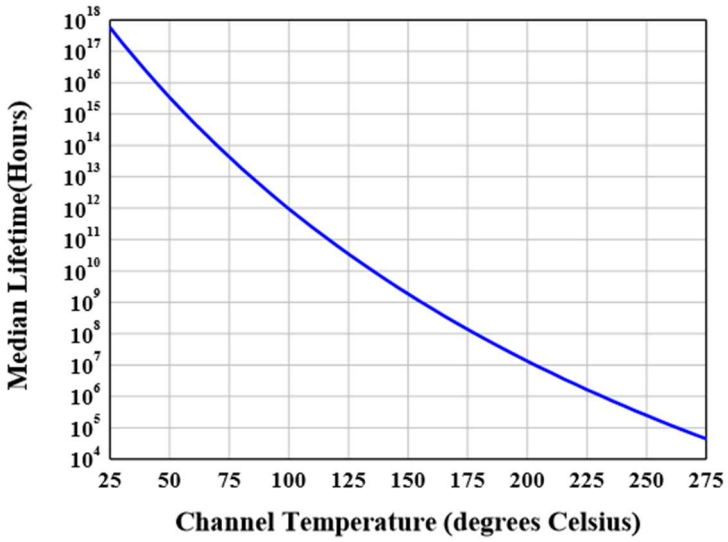


Figure 3: Efficiency and power gain as function of Pout

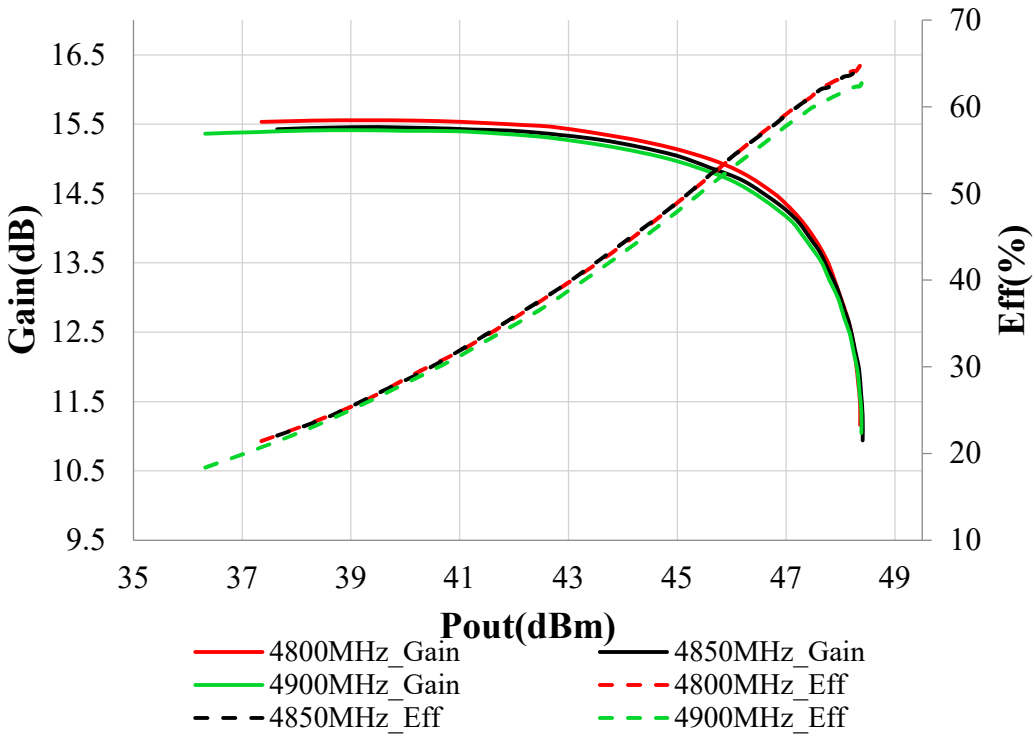


Figure 4: S11 / S21 output from network analyzer on 4.8-5GHz application board

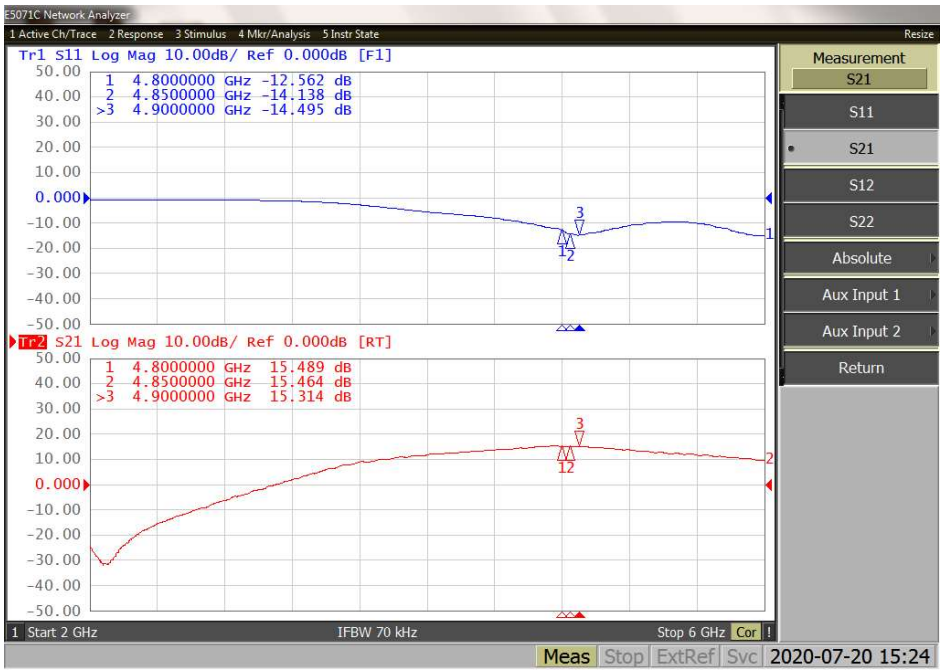
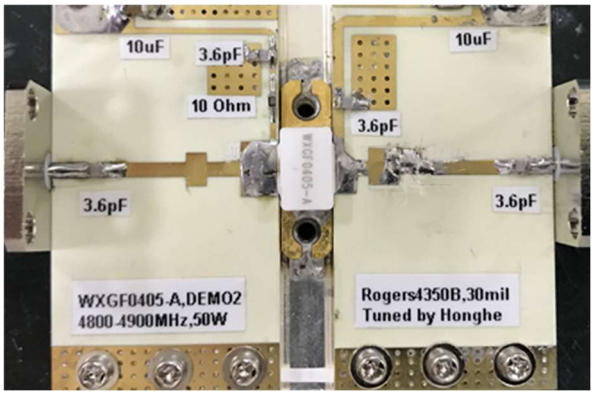
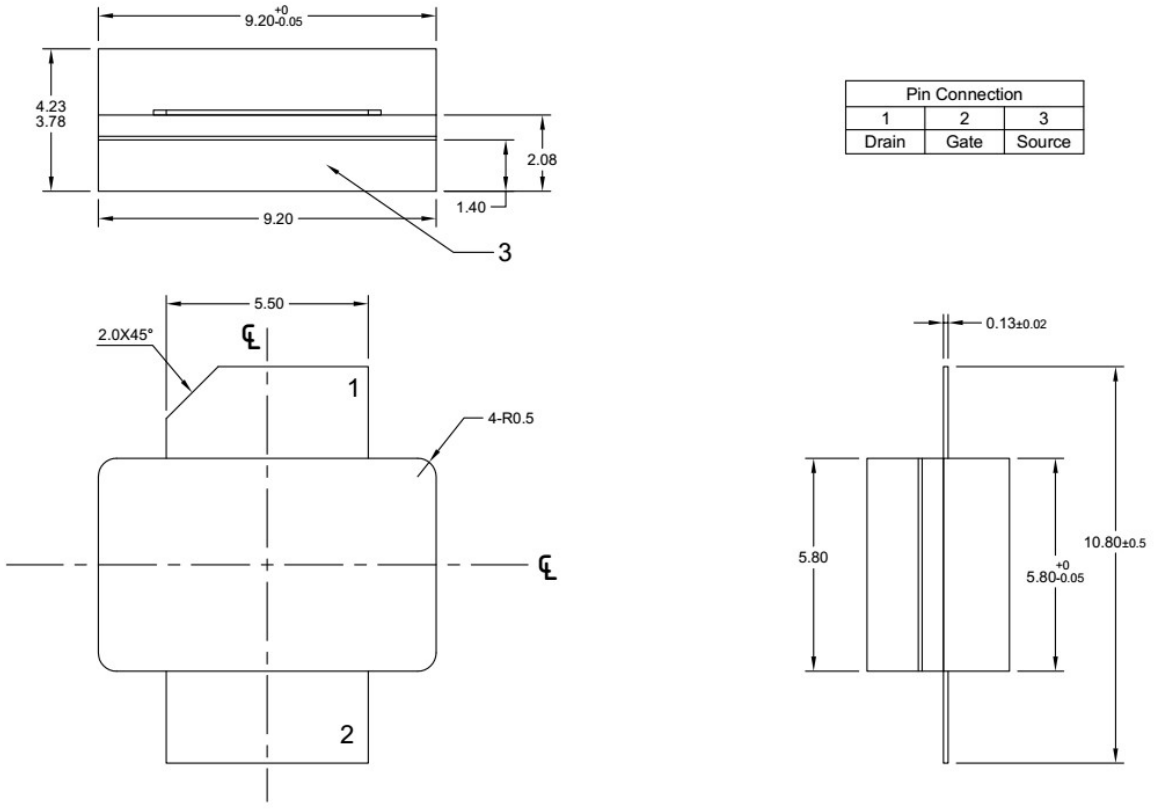


Figure 5: Picture of application board of 4.8-5GHz and bill of materials



Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB-2EL-9.2					2018.1.31

Figure 2. Package Outline PKG-G2

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2020/7/3	V1.0	Preliminary Datasheet Creation
2020/7/20	V1.1	Update based on new application board

Application data based on:ZHH-20-04

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