Document Number: STCV36500BY4V Preliminary Datasheet V1.0

Gallium Nitride 50V, 500W,3.3-3.6GHz RF Power Transistor

Description

The STCV36500BY4V is a 500-watt, internally matched GaN HEMT, designed for 5G cellular applications with frequencies from 3.3-3.6GHz, enabled by wide band VBW capability to support IBW ≥ 200MHz.

It can be configured as asymmetrical Doherty for 4G or 5G application, delivering 55 to 70W average power, according to normal 8 to 9dB back off.

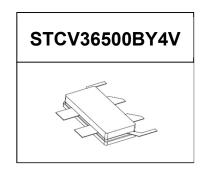
There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

VDD = 50 Vdc, IDQA = 280 mA, VGSB = -6 Vdc,

(1)Pulsed condition: 100us and 10%,

(2)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.



Freq	Pulse CW Signal(1)		Pavg=47.5dBm WCDMA Signal(2)		Pavg=48.5dBm WCDMA Signal(2)				
(GHz)	P1dB Gain	Psat	Psat	Cn (dP)	Eff(%)	ACPR5M	Cn (dP)	Eff(%)	ACPR5M
	(dB)	(dBm)	(W)	Gp (dB)	□ □ II(70)	(dBc)	Gp (dB)	□ □(1(70)	(dBc)
3.3	11.63	56.53	449.7	11.89	47.35	-34.76	11.89	49.97	-34.74
3.4	11.81	56.69	466.3	12.10	47.65	-33.49	12.10	50.19	-32.95
3.5	12.11	56.68	465.1	12.18	47.15	-35.95	12.18	49.21	-35.95
3.6	12.83	56.47	443.6	12.41	46.64	-35.42	12.41	48.73	-35.18

Applications

- Asymmetrical Doherty amplifier within N78 5G band and B42 4G band
- S band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

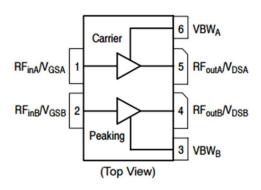
Turning the device ON

- 1. Set VGS to the pinch—off (VP) voltage, typically -5~V
- 2. Turn on VDS to nominal supply voltage
- 3. Increase VGS until IDS current is attained
- 4. Apply RF input power to desired level

Turning the device OFF

- 1. Turn RF power off
- 2. Reduce VGS down to VP, typically –5 V
- 3. Reduce VDS down to 0 V
- 4. Turn off VGS

Figure 1: Pin Connection definition



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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V _{DSS}	+200	Vdc
Gate—Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	22.4	Ма
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA	Rejc	1.2	°C /W
T _C = 85°C, Pout=70W, 3.6GHz Doherty application board	Kejc	1.2	C /VV

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=17Ma	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 17Ma	V _{GS(th)}	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=280Ma, Measured in Functional Test	$V_{GS(Q)}$		-3		V

DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=34Ma	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 34Ma	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=560Ma, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Load mismatch capability	3.6GHz, Pout=70W WCDMA 1					
	Carrier in Doherty circuit	VCMD		10.1		
	All phase,	VSWR		10:1		
	No device damages					



Figure 2: Intermodulation Distortion Products versus Two--Tone Spacing

Vdd=50V, Pout=47.5dBm, Center Frequency=3.5GHz

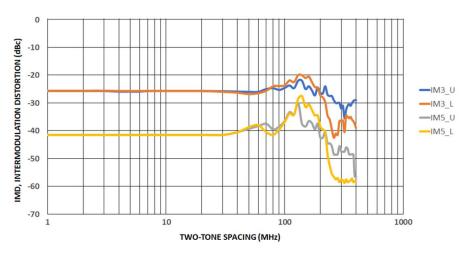


Figure 3: Efficiency and power gain as function of Pout (3.3-3.6GHz Doherty)

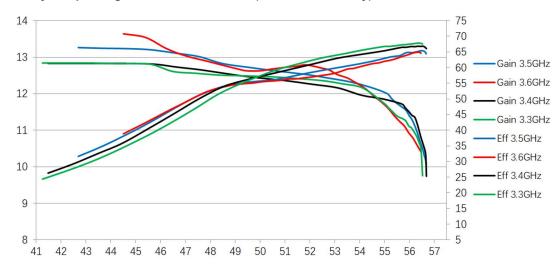


Figure 4: Network analyzer output, S11 and S21 (3.3-3.6GHz Doherty)



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Figure 5: Picture of application board Doherty circuit for 3.3-3.6GHz

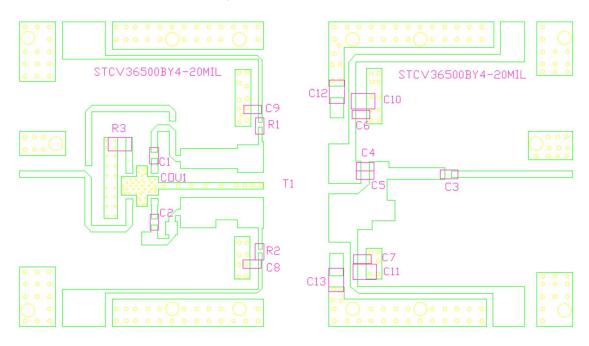


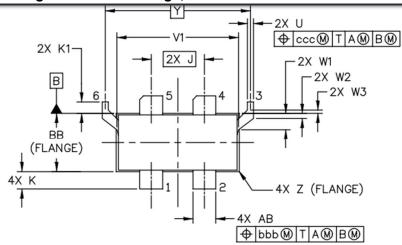
Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 30mils)

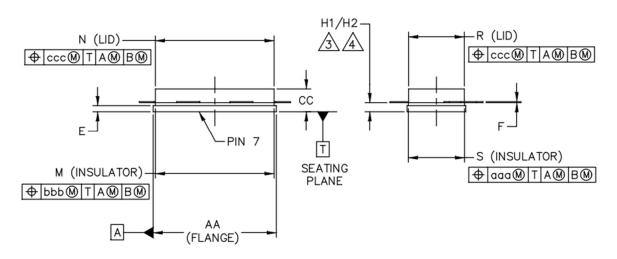
Table 4. Bill of mate	Table 4. Bill of materials of application board (1 Ob layout upon request, 10-4000b 3011115)						
Part	Quantity	Description	Part Number	Manufacture			
C1,C2,C3,C6,	7	8.2pFHigh Q	251SHS8R2BSE	TEMEX			
C7,C8,C9		Capacitor					
C4	1	2.0pFHigh Q	ATC600F2R0	ATC			
		Capacitor					
C5	1	2.0pFHigh Q	2.0pFHigh Q ATC600F2R0				
		Capacitor					
C10,C11,C12,C13	4	10uF MLCC	GRM32EC72A106ME05	Murata			
R1,R2	2	10 Ω Power Resistor	MCR10EZHJ100	ROHM			
R3	1	51 Ω Power Resistor	S1206N	RN2			
COU1	1	3 dB Bridge	XC3500P-03S	ANAREN			
T1	1	500W GaN	STCV36500BY4VV	Innogration			
		Dual Transistor					



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Earless Flanged Ceramic Package; 6 leads- BY4V





	IN	CH	MILLIN	METER		IN	CH	MILLIM	ETER
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
Ε	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.0975	.1175	2.48	2.98
H1	.057	.067	1.45	1.70	W2	.0225	.0425	0.57	1.08
H2	.054	.070	1.37	1.78	W3	.0125	.0325	0.32	0.83
J	.350	BSC	8.89	BSC	Υ	.956 BSC		24.28 BSC	
K	.0995	.1295	2.53	3.29	Z	R.000	R.040	R0.00	R1.02
K1	.070	.090	1.78	2.29	AB	.145	.155	3.68	3.94
М	.774	.786	19.66	19.96	aaa	.005		0.1	3
Ν	.772	.788	19.61	20.02	bbb	.010 0.25		25	
					ccc	.015		0.3	88



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Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/5/18	V1.0	Preliminary Datasheet Creation

Application data based on LWH-22-14

Notice

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