1800-2200MHz, 150W, 28V High Power RF LDMOS FETs

Description

The MK2215S is a 150-watt, internally matched LDMOS FETs, designed for wideband applications with frequencies at 1800 to 2200MHz.

It can be used in Class AB/B and Class C for all pulsed and CW formats.

• Typical Performance (on wideband board with device soldered):



Freq(MHz)	Pout(dBm)	Pout(W)	IDS(A)	Pin(dBm)	Gain(dB)	Eff(%)	2nd(dBc)
1800	52.43	175.0	11.4	42.82	9.61	54.82	27
1850	52.99	199.1	12.5	42.74	10.25	56.88	30.6
1900	53.19	208.4	12.7	42.96	10.23	58.62	28
1950	52.96	197.7	12.3	42.01	10.95	57.40	25.6
2000	53.07	202.8	12.5	41.99	11.08	57.93	24.3
2050	53	200	12.5	42.21	10.79	57.01	24.1
2100	53.04	201.4	12.6	42.92	10.12	57.08	25.6
2150	52.81	191.0	12.1	42.68	10.13	56.37	25
2200	52.11	162.6	11.2	42.5	9.61	51.84	28.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	mbol	١	/alue		Unit		
DrainSource Voltage	DSS	65					
GateSource Voltage	١	/ _{GS}	-10) to +10		Vdc	
Operating Voltage	١	/ _{DD}		+32		Vdc	
Storage Temperature Range	Т	stg	-65	to +150		°C	
Case Operating Temperature	-	Tc		+150		°C	
Operating Junction Temperature		TJ		+225		°C	
Table 2. Thermal Characteristics							
Characteristic	Syı	mbol	Value U				
Thermal Resistance, Junction to Case	ReJC 0.35				0 0 /W		
Case Temperature 80°C, DC Test	ĸ	юјс 0.35			°C/W		
Table 3. ESD Protection Characteristics		•			<u> </u>		
Test Methodology	Class						
Human Body Model (per JESD22A114)	Class 2						
Table 4. Electrical Characteristics (TA = 25 C u)	nless otherwise r	noted)					
Characteristic	Symbol	Min	Тур	Max	Unit		

DC Characteristics					
Zero Gate Voltage Drain Leakage Current				100	
(VDS = 65V, VGS = 0 V)	DSS			100	μA
Zero Gate Voltage Drain Leakage Current					•
(VDS = 28 V, VGS = 0 V)	I _{DSS}			1	μΑ
GateSource Leakage Current					
(VGS = 6 V, VDS = 0 V)	I _{GSS}			1	μΑ
Gate Threshold Voltage	N. and		2		v
(VDS =28V, ID = 300 μA)	V _{GS} (th)		2		v
Gate Quiescent Voltage			2.58		V
(VDD = 32 V, ID = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.50		v
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} =	28Vdc, I _{DQ} = 2	200 mA, f = 220	0 MHz		
VSWR 5:1 at 150W Pulsed CW Output Power	No Device Degradation				

TYPICAL CHARACTERISTICS

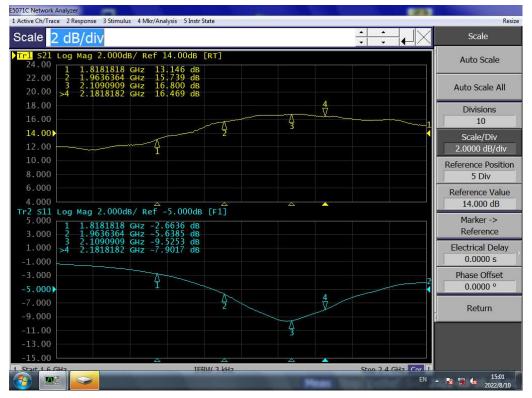
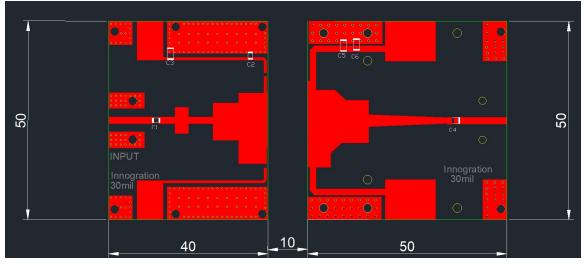


Figure 1. Network analyzer output S11/S21, Idq=1.5A, Vds=28V

Document Number: MK2215S Preliminary Datasheet V1.0

Reference Circuit of Test Fixture Assembly Diagram (Layout file upon request)

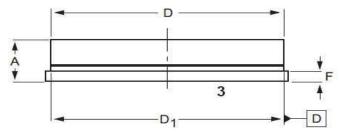


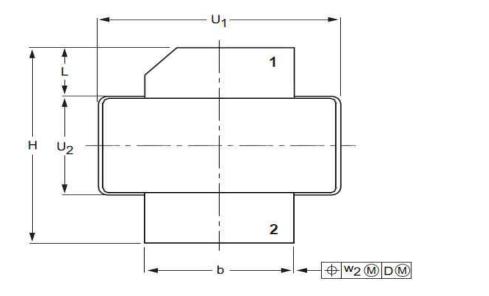
Component	Descripti	on	Suggested Manufacturer			
C1、C2	47PF	MQ200805	Beijing YN			
C4	39pF	MQ300709C0G2H390JNVB	Beijing YN			
C3、C6	10UF	1210				
РСВ	30mil Rogers4350B					

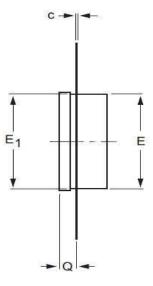
Document Number: MK2215S Preliminary Datasheet V1.0

Package Outline

Earless flanged ceramic package; 2 leads







0 5 10 mm ______scale

UNIT	A	b	с	D	D1	E	E1	F	Н	L	Q	U1	U_2	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	0.20
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	0.010

OUTLINE		REFE	RENCE	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION		
PKG-B2						03/12/2013	

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/8/10	Rev 1.0	Preliminary Datasheet Creation

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