

# SX1564RVP GaN TRANSISTOR

Document Number: SX1564RVP  
Preliminary Datasheet V2.1

## Gallium Nitride 50V, 640W, RF Power Transistor

### Description

The SX1564RVP is a 640-watt, unmatched GaN HEMT in form of push-pull configuration, designed for general purposes and wide band amplifier applications with frequencies from HF to 1500 MHz. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.



#### •Typical Performance (On Innogrator broadband application board):

$I_{DQ} = 130 \text{ mA}$ , Pulsed CW

Freq(MHz)	Drain Voltage(V)	Psat(W)	Gain(dB)	Eff(%)
30-678	50	400-550	17.6-20.9	51-62
30-678	28	160-220	15-18.5	56-71

#### •Typical Performance (On Innogrator broadband application board):

$I_{DQ} = 230 \text{ mA}$ , Pulsed CW

Freq(MHz)	Drain Voltage(V)	Psat(W)	Gain(dB)	Eff(%)
300-800	50	500-650	14.5-19.5	60-75

### Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically  $-5 \text{ V}$
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically  $-5 \text{ V}$
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to 0	Vdc
Operating Voltage	$V_{DD}$	0 to 55	Vdc
Maximum forward gate current	$I_{gf}$	79.2	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	C
Case Operating Temperature	$T_C$	-55 to +150	C
Operating Junction Temperature	$T_J$	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC Power Dissipation, FEA	$R_{\theta JC}$	0.44	C/W

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Preliminary Datasheet V2.1

**Table 3. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

**DC Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}; I_{DS} = 79.2\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}, I_D = 79.2\text{mA}$	$V_{GS(th)}$		-3.4		V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}, I_{DS} = 200\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.4		V

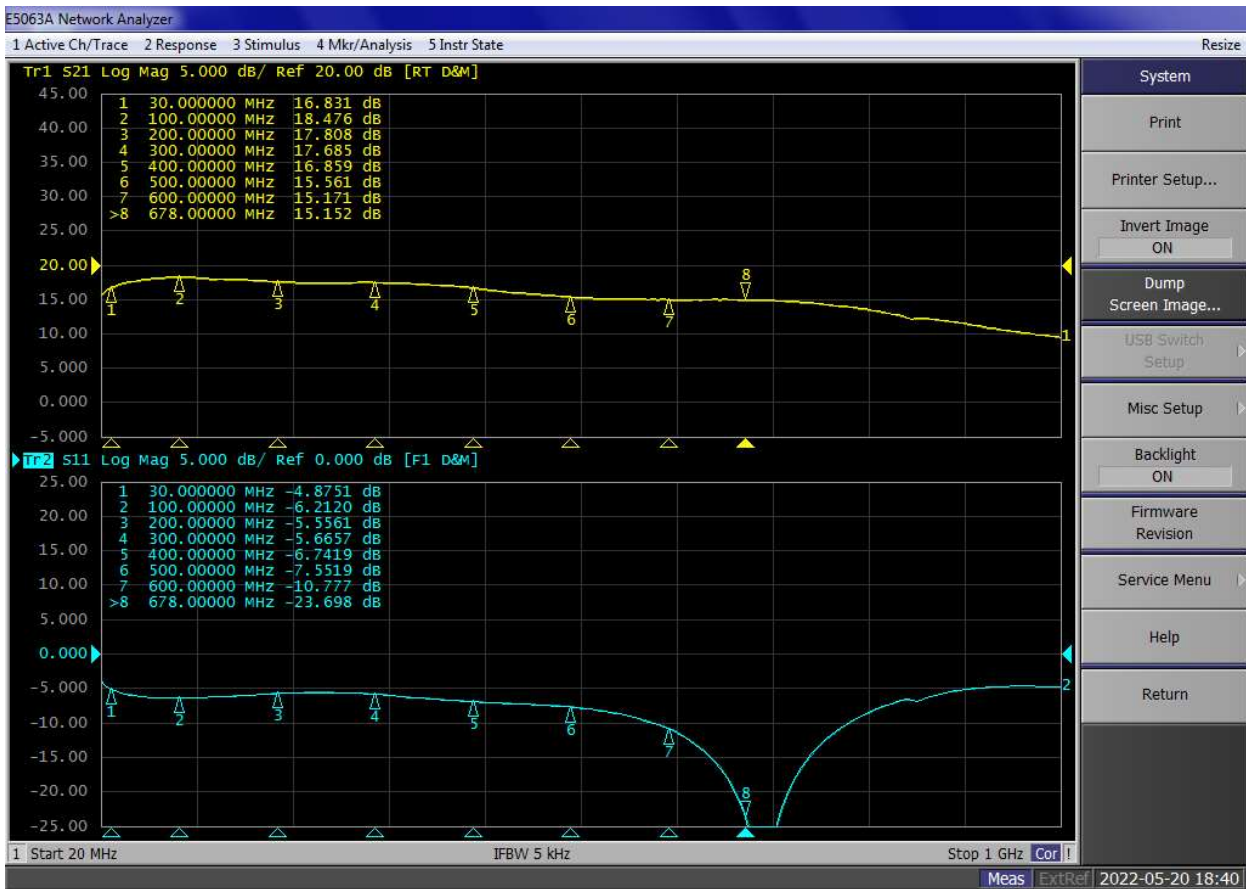
**Functional Tests (In Innogration narrow band production Test Fixture, 50 ohm system) :**  $V_{DD} = 48\text{Vdc}$ ,  $I_{DQ} = 200\text{ mA}$ ,  $f = 1000\text{ MHz}$ , CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P3dB	Gp		18		dB
Drain Efficiency@P3dB <sub>t</sub>	Eff		65		%
3dB Compressed point	P3dB		640		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		$\Psi$

## 30-678MHz

**Figure 2. Network analyzer output S11/S21 30-678MHz application board**

**$V_{DS} = 50\text{V}$   $I_{DQ} = 200\text{mA}$**



# SX1564RVP GaN TRANSISTOR

Document Number: SX1564RVP  
Preliminary Datasheet V2.1

Figure 3. Test Circuit Component Layout

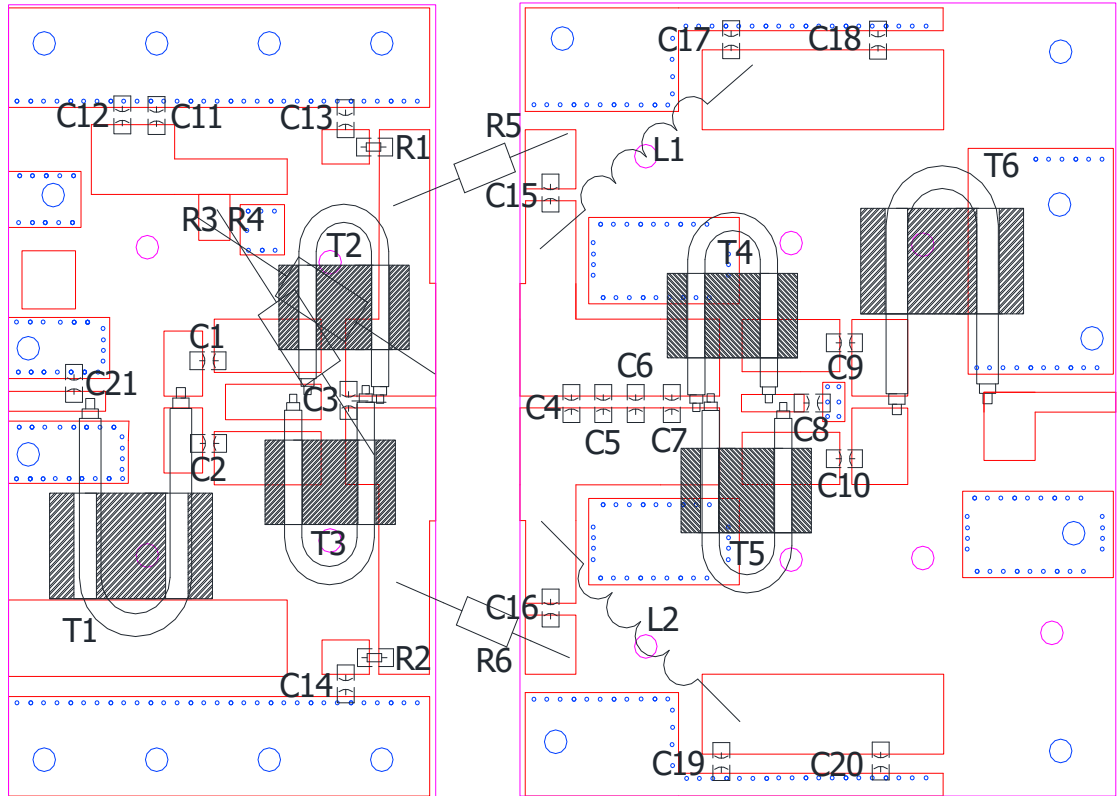


Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested types
C1,C2	150pF	MQ101111M7G2H151NMB
C9,C10,C15,C16	10nF	1812
C3	8.2pF	MQ101111M7G2H8R2NMB
C4,C6	5.6pF	MQ101111M7G2H5R6NMB
C5	3.3pF	MQ101111M7G2H3R3NMB
C7	3pF	MQ101111M7G2H3R0NMB
C11	200pF	ATC100B
C17,C19	470pF	MQ101111M7G2H470NMB
C21	0.8pF	ATC600F
C8,C12,C13,C14,C18,C20	10uF	10uF/50V
R1,R2	27Ω	0805
R3,R4	300Ω	3W/300Ω
R5,R6	200Ω	
T1,	50Ω,62mm	RG-047-1,BN-61-2402
T2,T3	17Ω,62mm	SFF-17-1.5,BN-61-202
T4,T5	17Ω,55mm	SFF-17-1.5,BN-61-202
T6	50Ω,62mm	SF-086-50,FB-61-5623
L1,L2	80nH	自制
PCB	30Mils, Roger4350B	

# SX1564RVP GaN TRANSISTOR

Document Number: SX1564RVP  
Preliminary Datasheet V2.1

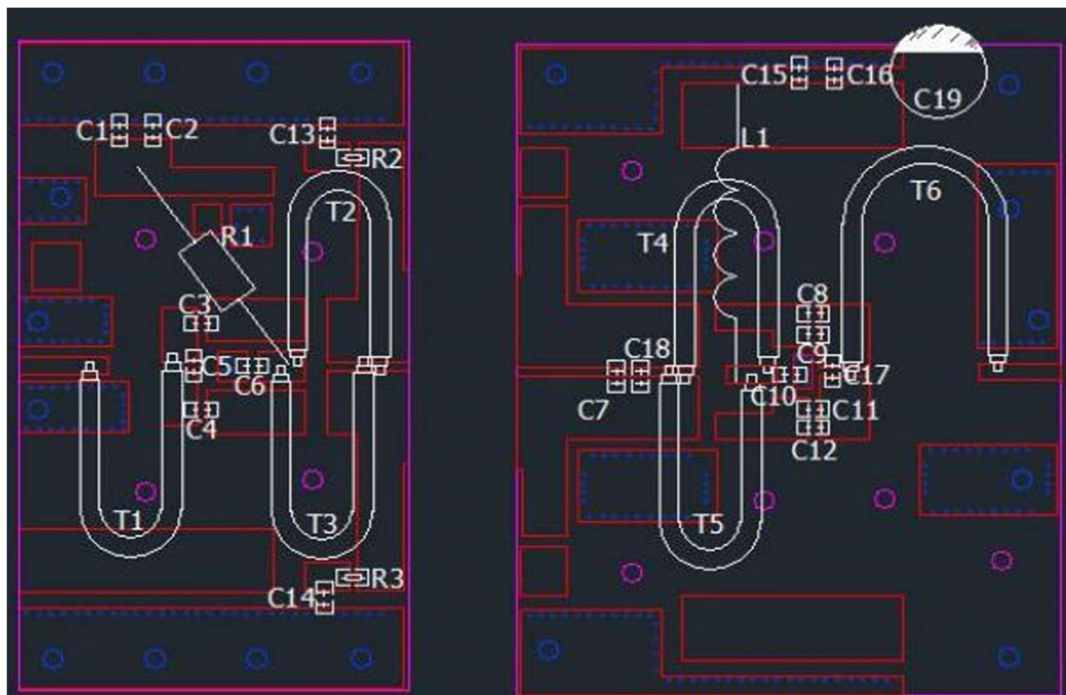
## 300-800MHz

Figure 4. Network analyzer output S11/S21 300-800MHz application board

VDS=50V IDQ=230mA



Figure 5. Test Circuit Component Layout



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Document Number: SX1564RVP  
Preliminary Datasheet V2.1

**Table 5. Test Circuit Component Designations and Values**

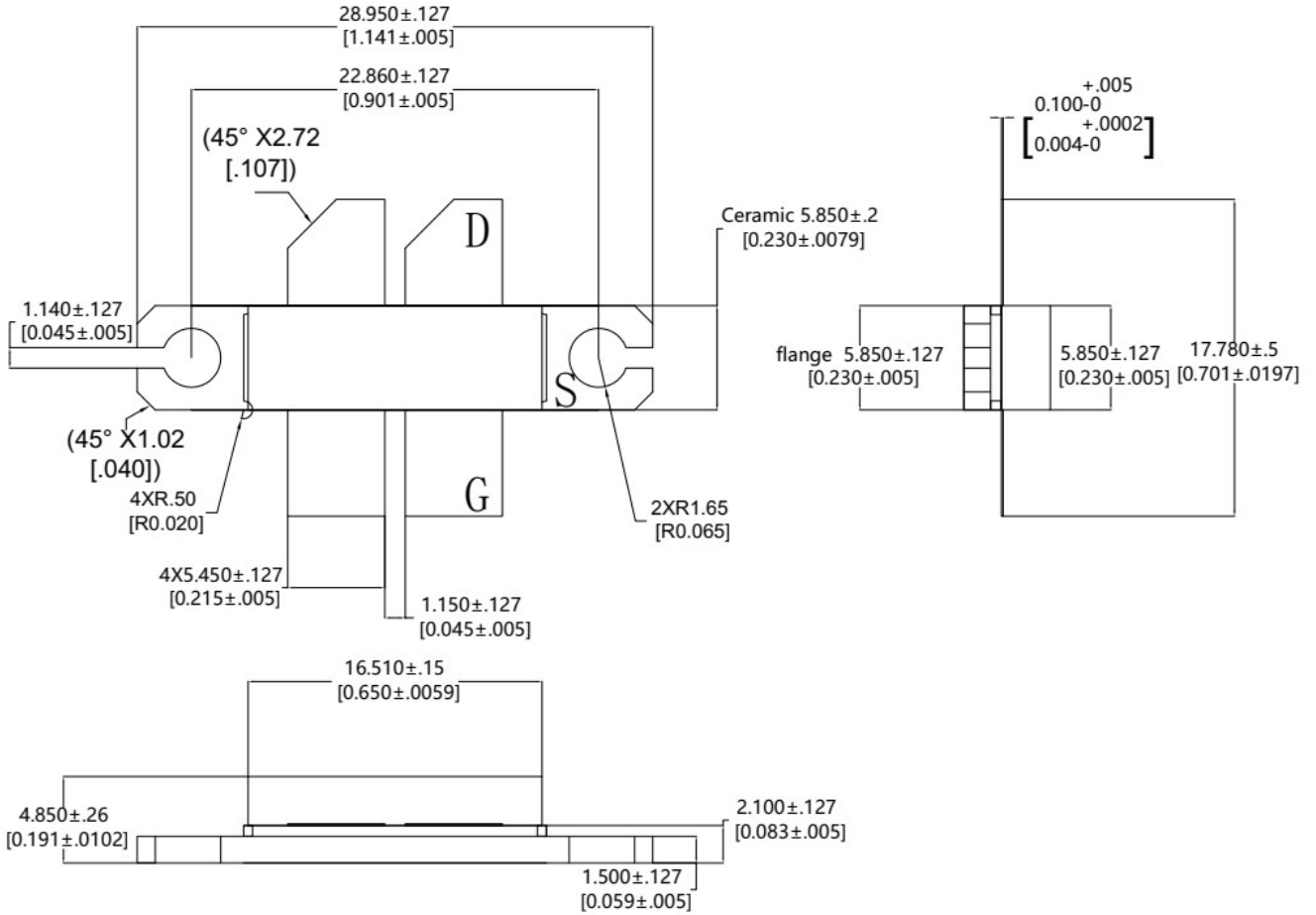
Part	description	Model
C2,C8,C9,C11,C12,C15	200pF	DLC70B
C5	4.7pF	DLC75D
C6,C10	10nF	Ceramic multilayer capacitor
C7, C18	8.2pF	DLC70B
C17	2pF	DLC75D
L1	11turns , 绕径 3mm	
C1,C13,C14,C16	10uF	Ceramic multilayer capacitor
C3,C4,	200pF	DLC75D
C19	4700uF/63V	Electrolytic Capacitor
R1	270ohm*2	
R2,R3	Chip Resistor, 5.1ohm	1206
T1,T6	50ohm, 60mm	SF-086-50
T2,T3	17ohm, 60mm	SFF-17-1.5
T4,T5	17ohm, 75mm	SFF-17-1.5

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Preliminary Datasheet V2.1

## Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					05/21/2021

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Preliminary Datasheet V2.1

## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2019/07/26	Rev 1.0	Preliminary Datasheet
2022/5/23	Rev 2.0	Update based on R suffix added and new 30-678MHz application data
2022/8/5	Rev 2.1	Add 300-800MHz application data

Application data based on ZL-21-14/ZL-22-10, TC-22-01

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