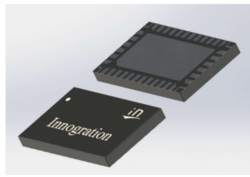
5.9-6.1GHz, 35W, 50V GaN fully matched PA Module

Description



The SMAV5961-35 is a 35-watt, integrated 2-stage Power Amplifier Module, designed for 5G massive MIMO applications, with frequencies from 5.9 to 6.1GHz. The module is 50 Ω input and output fully matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions，with much less sensitivity for production, housed in 10*6mm cost effective plastic open cavity package. The module incorporates a Doherty circuit delivering high power added efficiency for the entire module at 5.6 average power.

Innogration owns the patents for internal Doherty architecture, and related plastic open cavity.

• Typical 1 Carrier WCDMA Performance of Doherty Demo (On Innogration fixture with device soldered):

VDS= 50V, Idq1=10mA, Idq2=22mA,Vpeak=-4.9V				
Pout=37.5dBm				
Freq (MHz)	Ppeak(dBm)	ACPR (dBc)	Gain（dB）	EFF (%)
5900	45.93	-30.7	23.3	37.8
6000	45.88	-31.4	23.2	37.7
6100	45.7	-32	23.1	37.6

• Notes:

(1) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Features

- Industry leading RF performance for 5G MIMO AAU running at 6GHz, for instance
  - ✓ 64T:200W/ 200MHz
- Plastic open cavity without molding compound brings advantage compared to molded design
  - ✓ Minimize the risk of high density thermal distribution in fanless system for longer life time
  - ✓ Highly consistent RF performance for yield of volume production
- 50 Ω Input/output matched,
- Integrated Doherty Final and driver Stage
- 6x10 mm Surface Mount Package, full copper flange underneath for grounding and heat dissipation
- **When biased as Class AB, it can be extended as 5-6GHz 35W PA as well**

Pin Configuration and Description

Pin No.	Symbol	Description
1	VD1	Driver Amplifier, Drain Bias
3	VG1	Driver Amplifier, Gate Bias
6	RF IN	RF Input
11	VG3	Carrier Amplifier, Gate Bias
16	BE	VBW Enhance
22	RF OUT	RF Output
27	VD2	Peaking Amplifier, Drain Bias
32	VG2	Peaking Amplifier, Gate Bias
4,8-10,14-15,17,19,21,24,26,28,29,33-35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36	GND	Internal Grounding, recommend connecting to Epad ground
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.6	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case Tcase=+85℃，CW Test，，Pout=5.6W,	$R_{\theta JC}$	TBD	°C/W

Notes:

(1) The thermal resistance is acquired by our company's FEA model,which was calibrated by IR measurement,the value shall be applied to reliability.

(2) The reference Tcase temperature 85℃ is apply on the backside of package.

(3) If the device soldering onto the 20mil Rogers PCB with 50×Φ0.4mm via hole beneath the package backside and the reference temperature Tcase（85℃） apply on the groundside of the PCB, the total thermal resistance RθJC (TBD)℃/W.

(4) The power dissipation in the table is overall dissipation which include Carrier PA, Peaking PA and driver PA.

Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	TBD
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	±1000V

Table 4:Load Mismatch Characteristics (On Test Fixture, 50 ohm system): f = 6.0 GHz

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

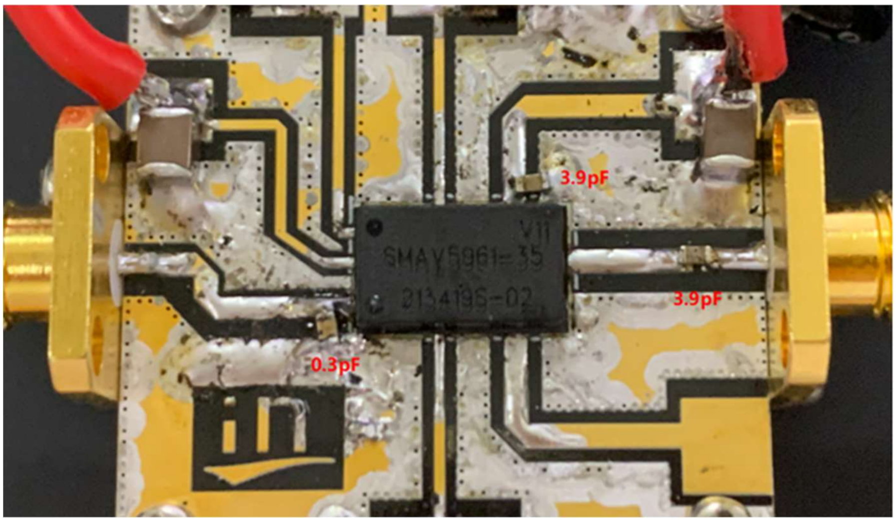


Figure 1. Test Circuit Component Layout

TYPICAL CHARACTERISTICS

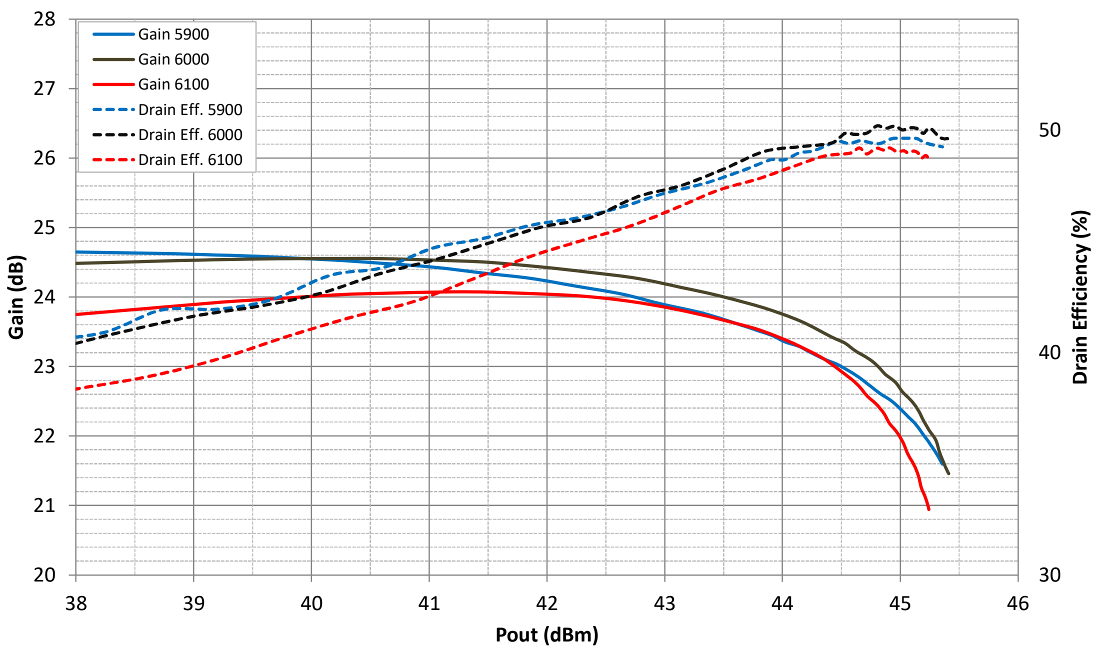


Figure 2. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power

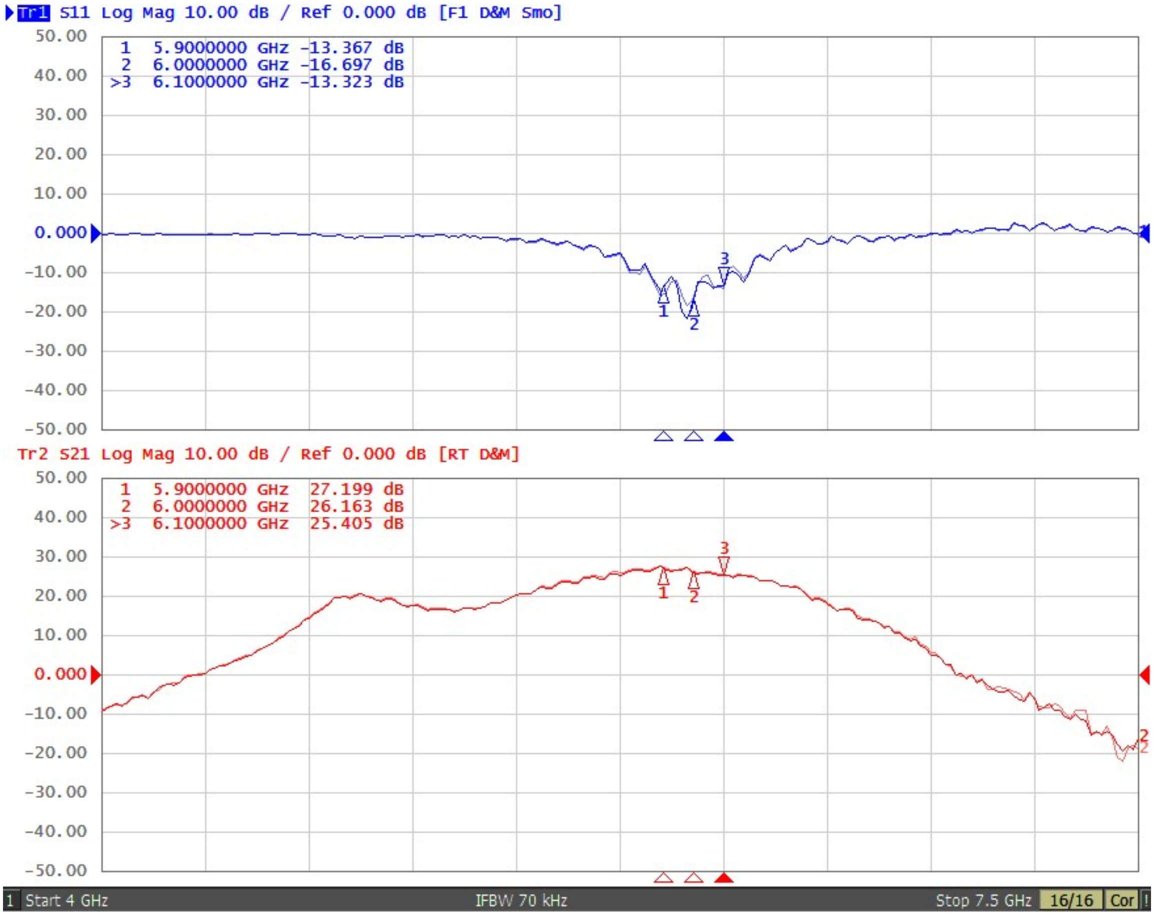
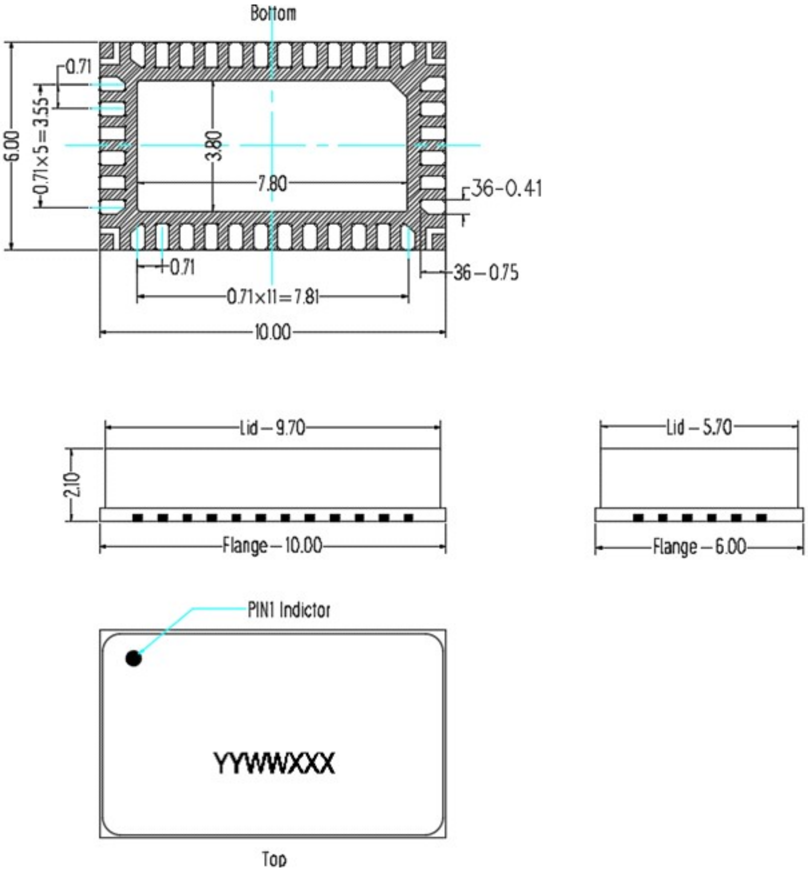


Figure 3. Network analyzer output, S11/S21

Package Dimensions

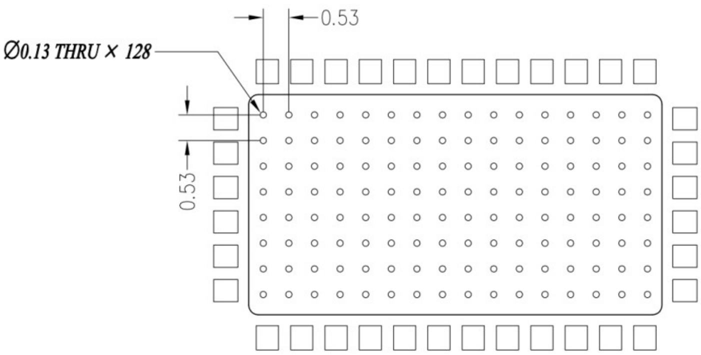
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/8/23	Rev 1.0	Preliminary Datasheet
2021/8/20	Rev 1.1	SMAV to SMBV and update according to latest application report
2022/9/10	Rev 1.2	Correct typo of pin definition, VG1 and RF OUT

Application data based on HJ-21-12

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