MX1512VP LDMOS TRANSISTOR

120W, 50V High Power RF LDMOS FETs

Description

The MX1512VP is a 120-watt, highly rugged, thermally enhanced, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

•Typical Performance (On Innogration narrow band fixture with device soldered):

 $V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA, CW.

Frequency	Gp (dB)	P _{out} (W)	η _D @P _{out} (%)
915 MHz	23	120	60

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift

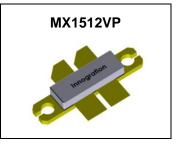
Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 1200-1400MHz(L band)

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz 1000MHz (ISM, instrumentation)
- 960-1215MHz(Avionics)

Table 1. Maximum Ratings

Rating	S	ymbol	Value	Unit	
DrainSource Voltage		V _{DSS}	+125	Vdc	
GateSource Voltage		V _{GS}	-10 to +10	Vdc	
Operating Voltage		V _{DD}	+55	Vdc	
Storage Temperature Range		Tstg	-65 to +150	°C	
Case Operating Temperature		Tc	+150	°C	
Operating Junction Temperature		TJ	+225	°C	
Fable 2. Thermal Characteristics				·	
Characteristic		Symbol	Value	Unit	
Thermal Resistance, Junction to Case		D		°C/W	
Γ_{c} = 85°C, Pout=120W CW,		Rejc	0.7		
Fable 3. ESD Protection Characteristics			· ·		
Test Methodology		Class			



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Human Body Model (per JESD22--A114)

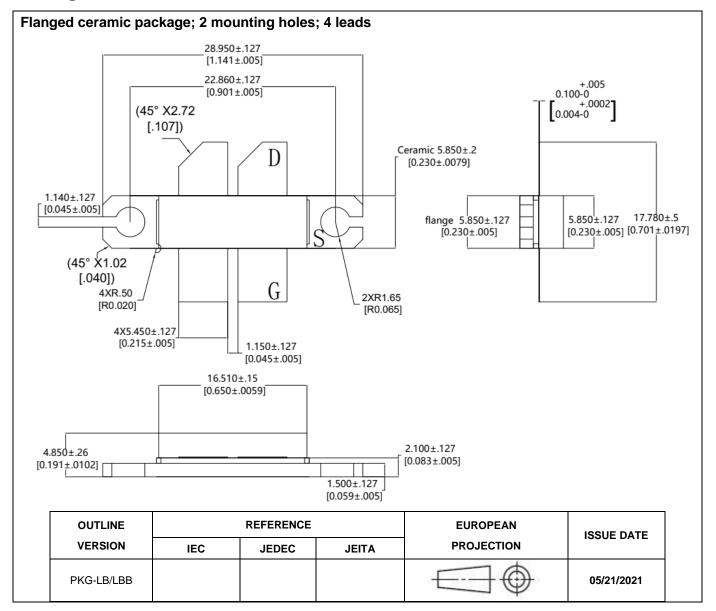
Class 2

Table 4. Electrical Characteristics (TA = 25 $\,^\circ\!\mathrm{C}\,$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics	·				
Drain-Source Voltage	N		400		M
V _{GS} =0, I _{DS} =1.0Ma	$V_{(BR)DSS}$		122		V
Zero Gate Voltage Drain Leakage Current					
$(V_{\text{DS}} = 50 \text{V}, V_{\text{GS}} = 0 \text{V})$	I _{DSS}			1	μΑ
Gate—Source Leakage Current					
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}			1	μA
Gate Threshold Voltage			0.05		
$(V_{DS} = 50V, I_D = 600 \ \mu A)$	V _{GS} (th)	V _{GS} (th)	2.65		V
Gate Quiescent Voltage	N		3.57		V
$(V_{\text{DD}}$ = 50 V, I_{D} = 400 mA, Measured in Functional Test)	$V_{GS(Q)}$				
Drain source on state resistance	Dele (ere)		448		
(V_{\text{DS}} = 0.1V, V_{\text{GS}} = 10 V) Each section side of device measured	Rds(on)				mΩ
Common Source Input Capacitance	C _{ISS}		55.5		pF
(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device					
measured					
Common Source Output Capacitance	C _{OSS}		22.6		pF
(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device					
measured					
Common Source Feedback Capacitance	C _{RSS}		0.57		pF
(V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device					
measured					
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vd	c, I _{DQ} = 100mA, f	= 915 MHz, C	N Signal Meas	surements, Pin	=22.5dBm
Power Gain@Pout	Gp		23		dB
Output Power	Pout		120		W
Drain Efficiency@Pout	η _P		60		%
Input Return Loss	IRL		-7		dB
Ruggedness at all phase angle	VSWR		10:1		

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Package Outline



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/15	Rev 1.0	Preliminary Datasheet Creation
2021/5/21	Rev 1.1	Package outline update

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