MX0540X LDMOS TRANSISTOR

Document Number: MX0540X
Product Datasheet V1.1

400W, 28V High Power RF LDMOS FETs

Description

The MX0540X is a 400-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 250MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

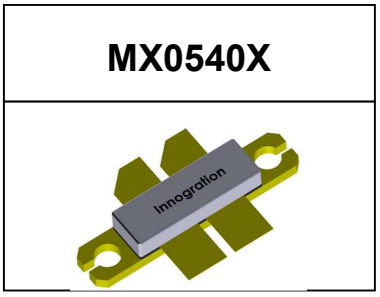


Figure 1. Pin Connection

•Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 2000 mA, CW.

Freq(MHz)	G_P (dB)	P_{-1dB} (W)	Eff(%)
250	17	380	70

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics (per half section)

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95	98		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 650 μA)	$V_{GS(th)}$	——	2.19	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 1.0 A, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		187		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		79		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		4.6		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 2000 mA, f =250 MHz, CW Signal Measurements.

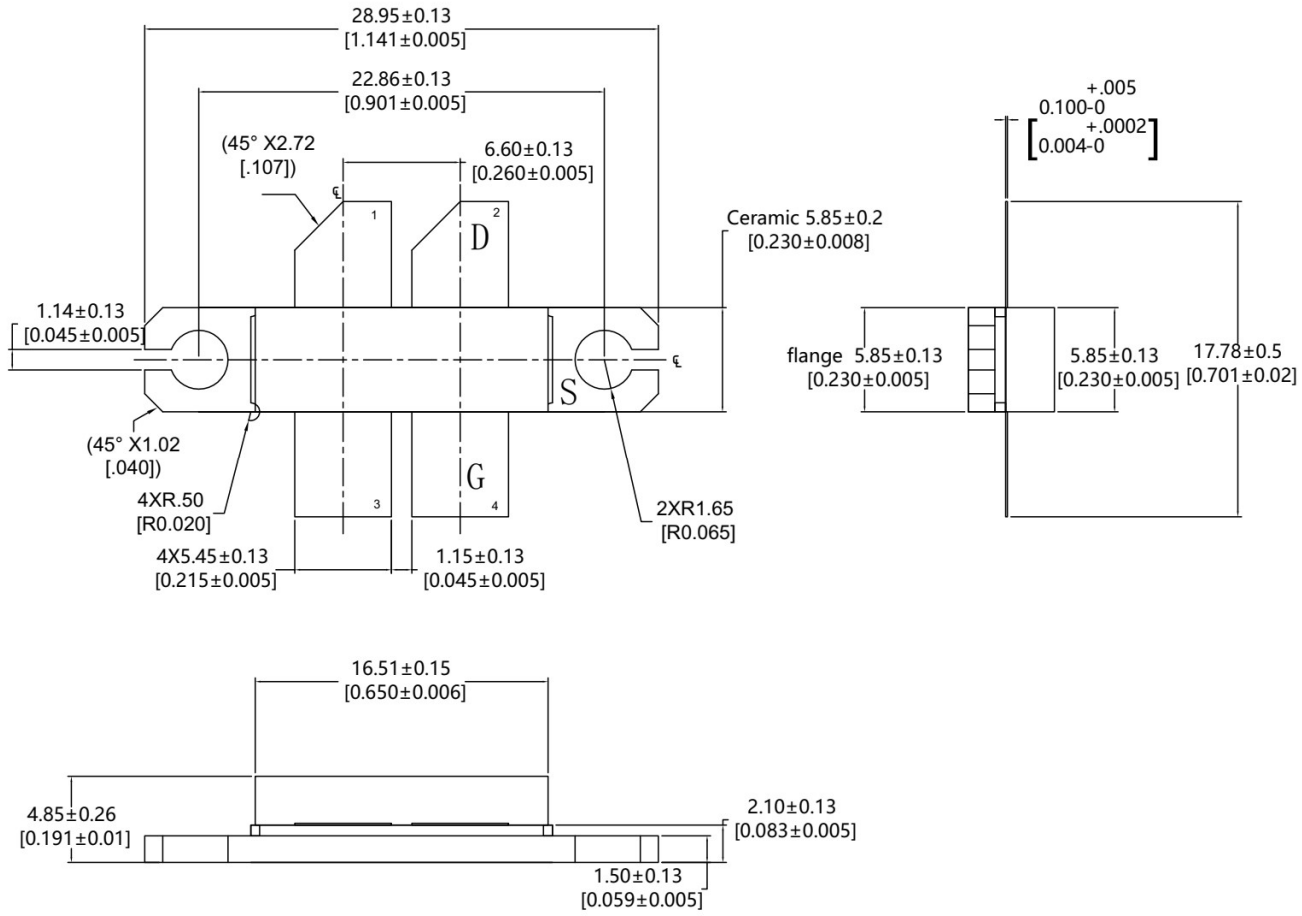
Power Gain	G_p	——	17	——	dB
Drain Efficiency@P1dB	η_D	——	70	——	%
1 dB Compression Point	P_{-1dB}	——	380	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 2000 mA, f = 250 MHz

VSWR 20:1 at 380W pulse CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					05/21/2021

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/03/13	Rev 1.0	Product Datasheet
2019/10/16	Rev 1.1	Modified to rugged version with X suffix ,modified upper frequency
2022/9/19	Rev 1.2	LBB Pkg outline updated

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