MJ1505 LDMOS TRANSISTOR

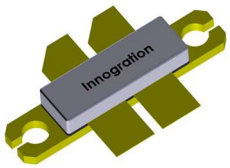
Document Number: MJ1505
Product Datasheet V2.1

50W, 28V High Power RF LDMOS FETs

Description

The MJ1505 is a 50-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

MJ1505



- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 300 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
1000 MHz	20	50	60

- Typical Performance (In Innogration broadband demo): V_{DD} = 12 Volts, I_{DQ} = 100 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)
20 MHz	15.1	41.0	50.1
30 MHz	14.9	41.6	53.0
100 MHz	15.5	41.4	50.7
200 MHz	17.1	42.1	62.7
300 MHz	17.1	42.3	64.5
400 MHz	16.6	42	63.0
500 MHz	15.6	41.4	61.6
600 MHz	15.6	40.2	54.8
700 MHz	16.0	39.7	51.2

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C

Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 150 μA)	$V_{GS(th)}$	——	2.17	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D =100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.9	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		30.7		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		13.4		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.7		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 300 mA, f = 1000 MHz, CW Signal Measurements.

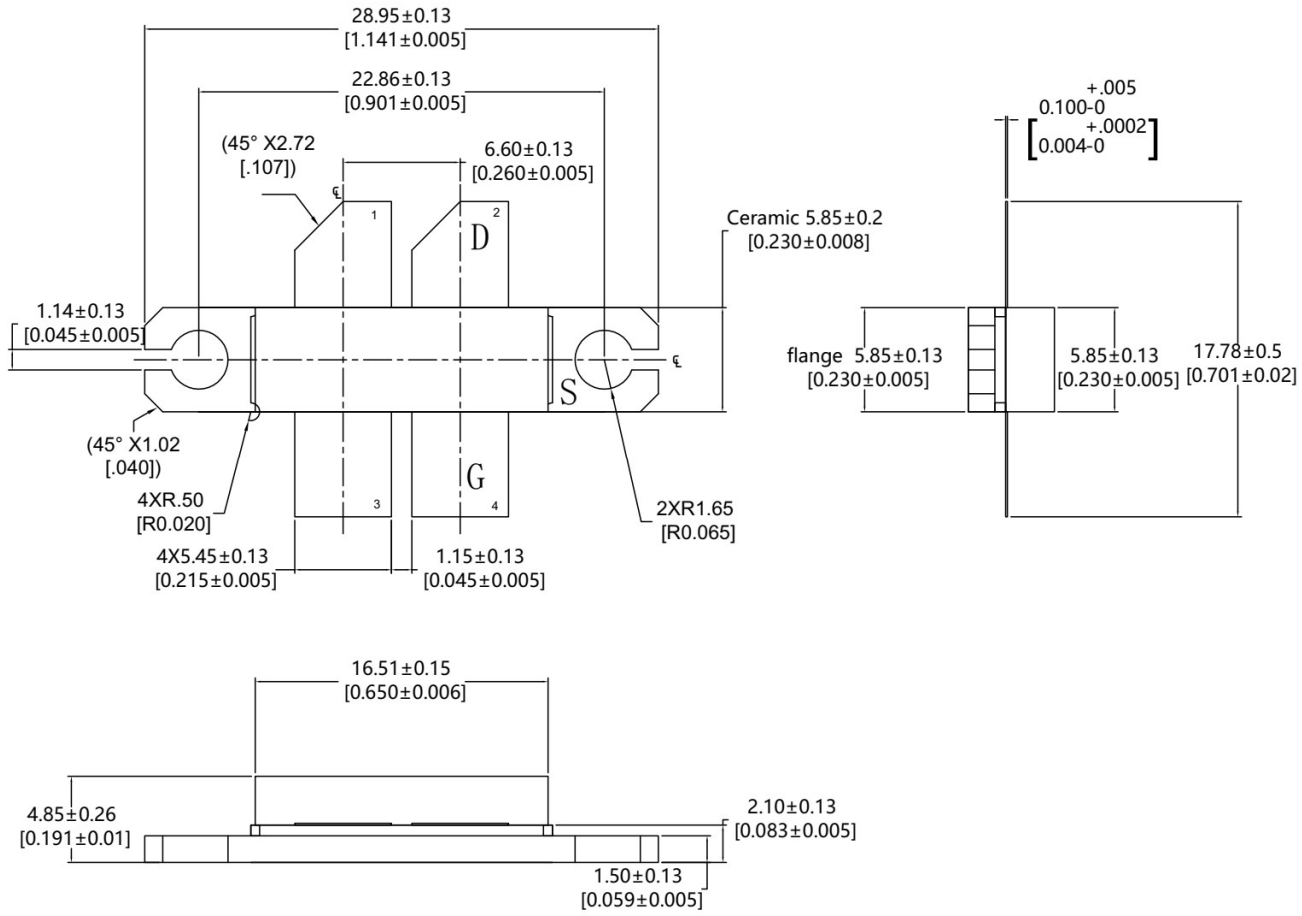
Power Gain	G_p	——	20	——	dB
Drain Efficiency@P1dB	η_D	——	60	——	%
1 dB Compression Point	P_{-1dB}	——	50	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 300 mA, f = 1000 MHz

VSWR 20:1 at 50W pulse CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					05/21/2021

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2016/8/8	**Rev 1.0**	**Preliminary Datasheet**
2016/12/27	**Rev 1.1**	**Preliminary Datasheet**
		Add Thermal Resistance
2017/02/20	**Rev 2.0**	**Product Datasheet**
2022/9/19	**Rev 2.1**	LBB outline updated

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