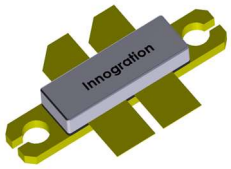
MX1516C LDMOS TRANSISTOR

Document Number: MX1516C
Product Datasheet V1.2

60W, 12.5V High Power RF LDMOS FETs

MX1516C



Description

The MX1516C is a 60-watt capable, highly rugged, unmatched,push pull LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 600MHz.

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 12 Volts, I_{DQ} = 800 mA, CW.

Freq(MHz)	Pin(dBm)	P3dB(dBm)	P3dB(W)	IDS(A)	Gain(dB)	Eff(%)
2	23.3	48.2	66	7.6	24.9	69.47%
5	22.6	48.2	66	7.5	25.6	70.40%
10	22.6	48.2	66	7.49	25.6	70.49%
15	23.5	48.15	65	7.55	24.65	68.87%
20	24.2	48.1	64	7.53	23.9	67.99%
25	24.5	48.1	64	7.7	23.6	66.49%
30	23.6	47.9	61	7.6	24.3	64.21%
35	25.2	47.8	60	7.73	22.6	62.10%
40	26.4	47.5	56	7.38	21.1	60.70%
45	27.4	47.7	58	7.86	20.3	59.03%
50	27.2	47.9	61	8.2	20.7	59.51%
54	28.2	48	63	8.39	19.8	60.07%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 100kHz - 100MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc

Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=60W,CW Test	RθJC	0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	65			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 12.5V, I_D = 400 μA)	$V_{GS}(th)$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 12.5 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.48	——	V

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 12.5Vdc, I_{DQ} = 200mA, f = 30MHz, CW Signal Measurements, Pin=23.6dBm

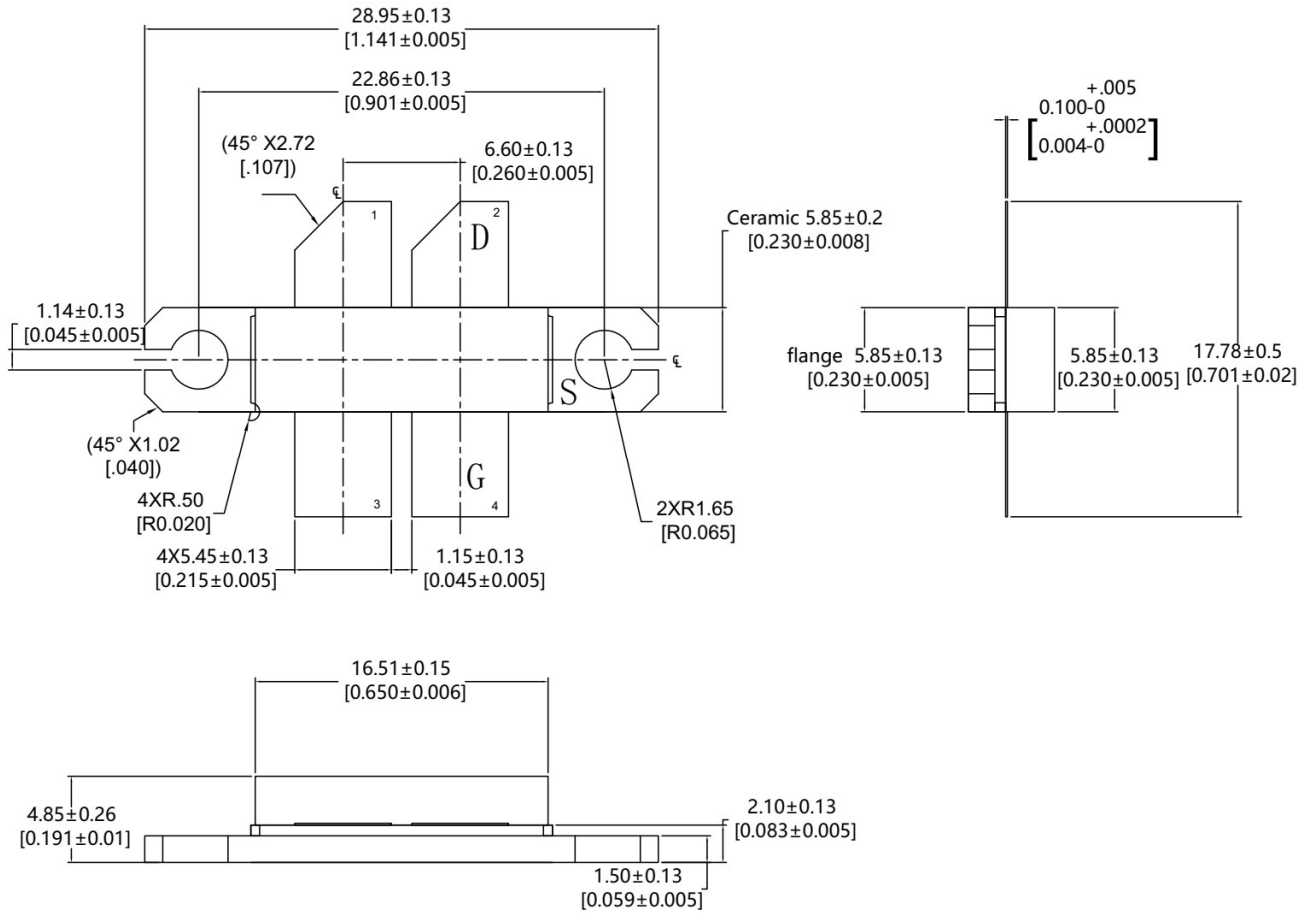
Power Gain	Gp	——	18	——	dB
Drain Efficiency@Pout	η_D	——	64	——	%
Output Power	P_{out}	——	60	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12.5 Vdc, I_{DQ} = 200 mA, f = 2 MHz

Load open and short, at 60W CW	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					05/21/2021

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/9/29	Rev 1.0	Product Datasheet Creation
2020/3/9	Rev 1.1	Modify typo on 1st page
2022/9/19	Rev 1.2	LBB Outline updated

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