



GaN HEMT 50V, 500W, 1.8-2.0GHz RF Power Transistor

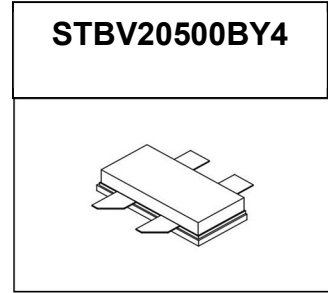
Description

The STBV20500BY4 is a dual path 500watt , Input matched GaN HEMT, ideal for applications from 1.8 to 2.0GHz especially for LTE/5G

- Typical WCDMA 1C performance on 1.8GHz asymmetrical Doherty with device soldered

Vds= 50V, Idq=150mA(Vgs_main=-3.06V, Vgs_peak=-5.3V)

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
1805	49.0	8.41	57.42	552.4	-28.1	16.8	61.0
1843	49.0	8.73	57.72	592.0	-29.1	16.9	61.8
1880	49.0	8.73	57.71	590.8	-31.4	16.4	61.0



Applications

- Asymmetrical Doherty amplifier within 1.8-2.0GHz
- Sub-2GHz power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

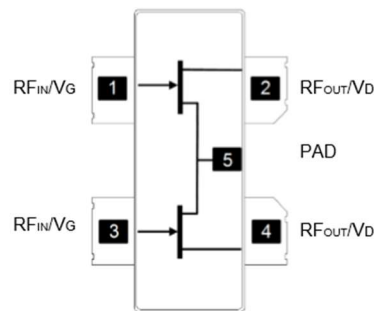


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	I _{gs}	65	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C



Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, at $P_d = 50\text{W}$, on Doherty application board	$R_{\theta JC}$	1.1	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 25\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 25\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 250\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.0		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 39.6\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 39.6\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 250\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.84GHz, $P_{out} = 80\text{W}$ WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

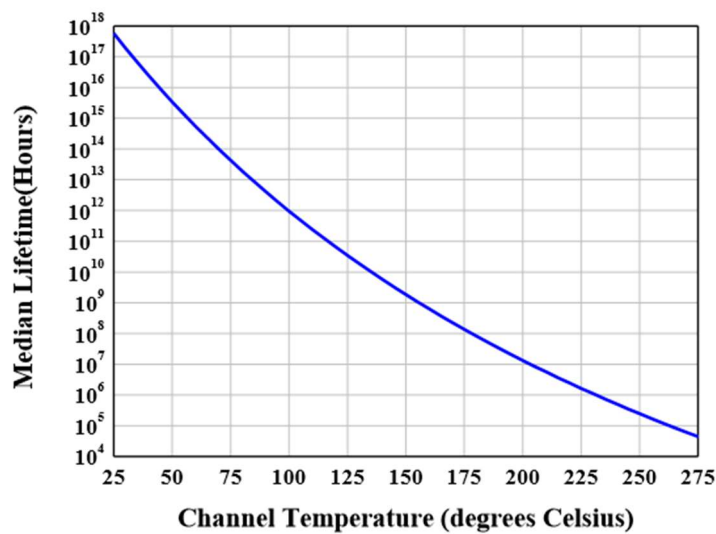




Figure 3: Efficiency and power gain as function of Pout (1.8GHz Doherty)

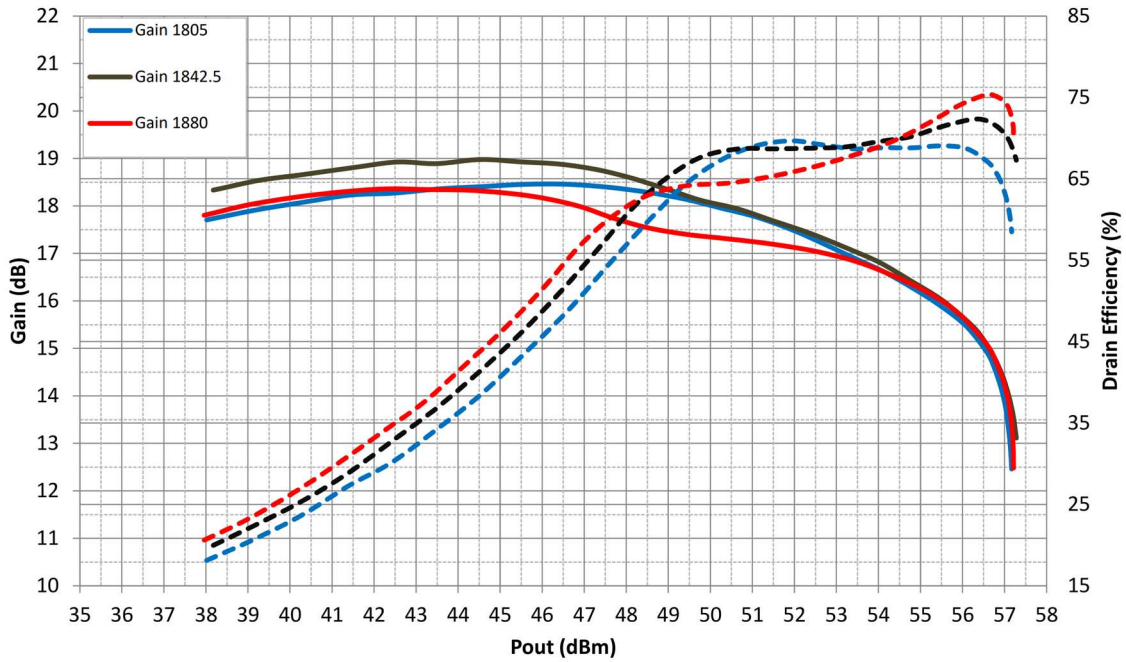


Figure 4: Network analyzer output, S11 and S21

m1 freq=1.805 GHz dB(S(2,1))=18.705 dB(S(1,1))=-14.782	m2 freq=1.843 GHz dB(S(2,1))=19.156 dB(S(1,1))=-13.558	m3 freq=1.880 GHz dB(S(2,1))=18.859 dB(S(1,1))=-12.309
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S-Parameters_STBV20500BY4 DHT

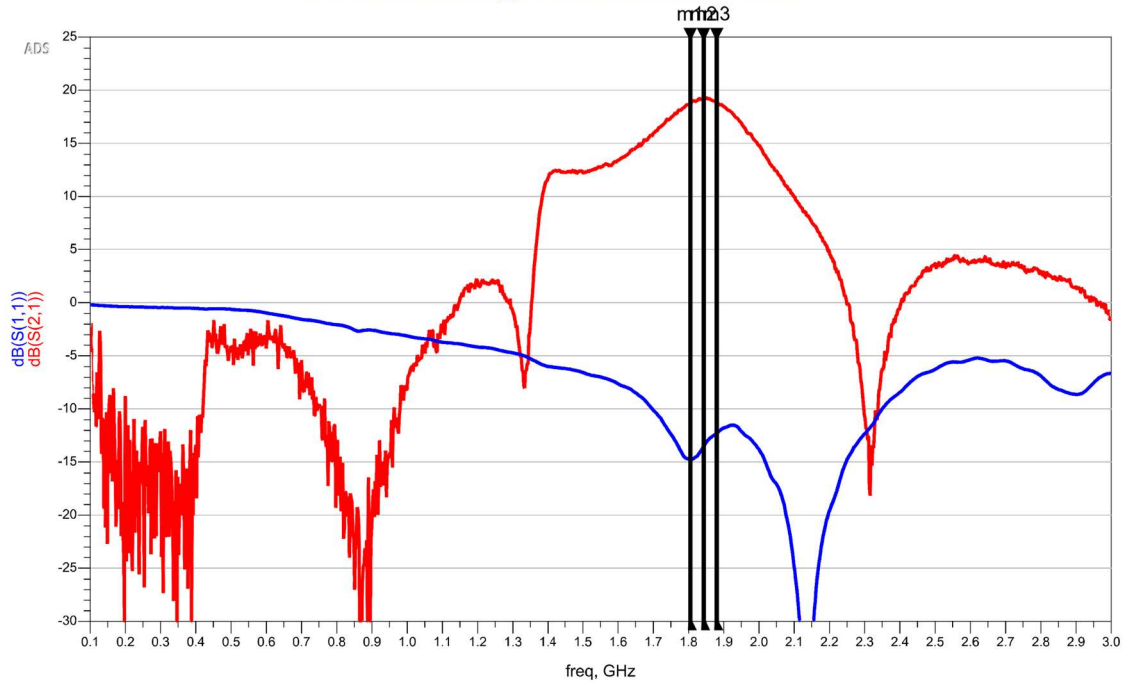


Figure 5: Picture of application board Doherty circuit for 1.8GHz

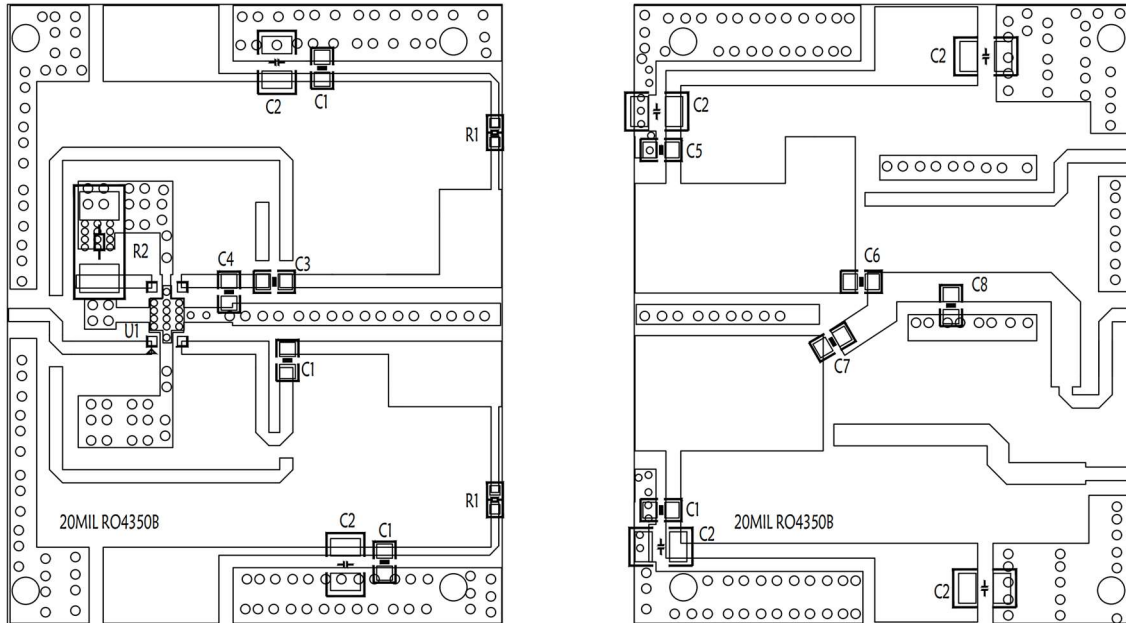
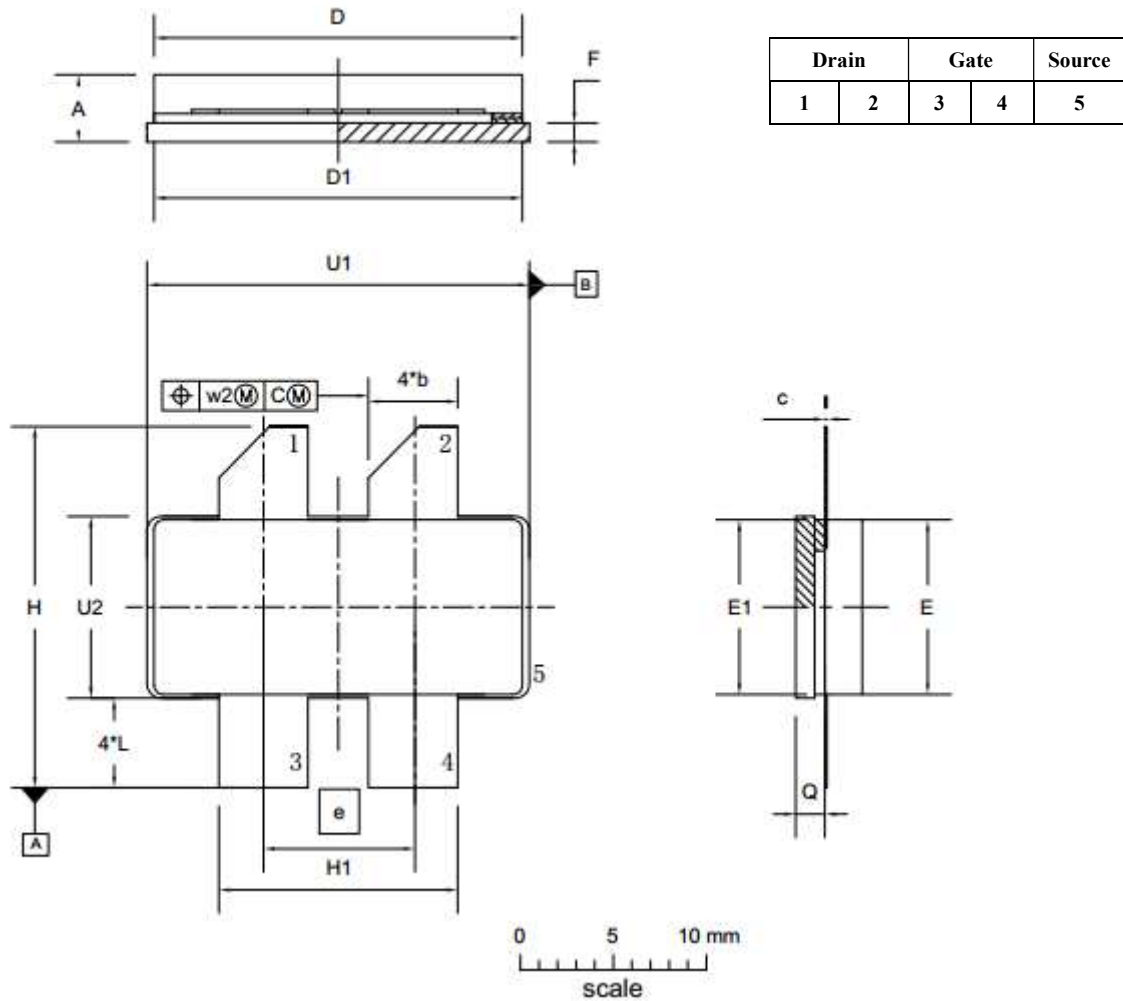


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1	0805	20pF/250V	4
C2	1210	10uF/100V	6
C3	0805	3.9pF/250V	1
C5	0603	15pF/250V	1
C6	0603	3.3pF/250V	1
C7	0603	20pF/250V	1
C8	0805	0.6pF/250V	1
R1	0603	10R	2
R2	2512	51R	1
U1	5.08*3.18mm	X3C20F1-02S	1



Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/8/5	V1.0	Preliminary Datasheet Creation

Application data based on: ZBB-22-03

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