



GaN HEMT 50V, 500W, 2.1-2.2GHz RF Power Transistor

Description

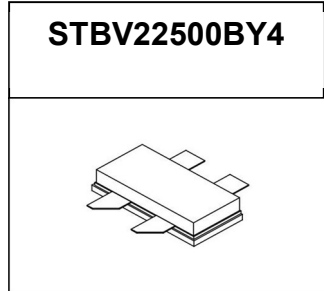
The STBV22500BY4 is a dual path 500watt , Input matched GaN HEMT, ideal for applications from 2.1 to 2.2GHz especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=150mA(Vgm=-3.07V, Vgp=-5.50V)

Pulsed CW: 20uS width, 10% cycle.



Freq (MHz)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)	P3dB Gain(dB)	P5dB (dBm)	P5dB (W)	P5dB Eff(%)
2110	56.27	423.64	67.52	14.51	57.37	545.14	63.24
2140	55.94	392.64	69.39	14.73	57.26	532.07	66.97
2170	55.84	383.71	71.06	14.50	57.15	518.80	70.14

WCDMA 1 carrier performance

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2110	49	7.72	-26.44	15.79	60.25
2140	49	7.68	-27.26	15.75	60.12
2170	49	7.56	-28.51	15.37	59.25

Recommended driver:

- Class AB (1 stage discrete solution): STAV38041C6

Applications

- Asymmetrical Doherty amplifier within 2.1-2.2GHz
- S band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

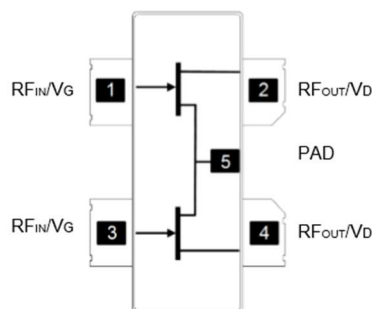




Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	61	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, at $P_d = 105\text{W}$, on Doherty application board	$R_{\theta JC}$	1	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 25.2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 25.2\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 150\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.07		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 39.6\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 39.6\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 150\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.0		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.14GHz, $P_{out} = 90\text{W}$ WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

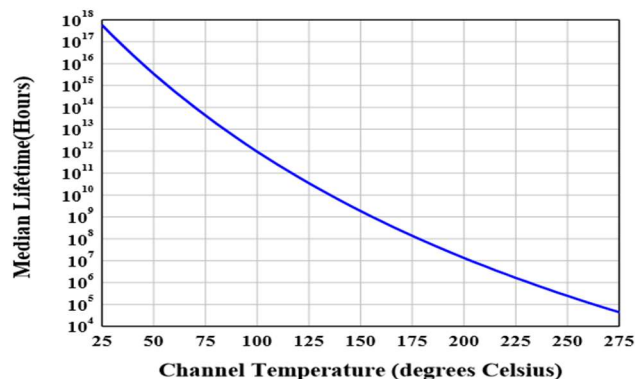




Figure 3: Efficiency and power gain as function of Pout (2.1-2.2GHz Doherty)

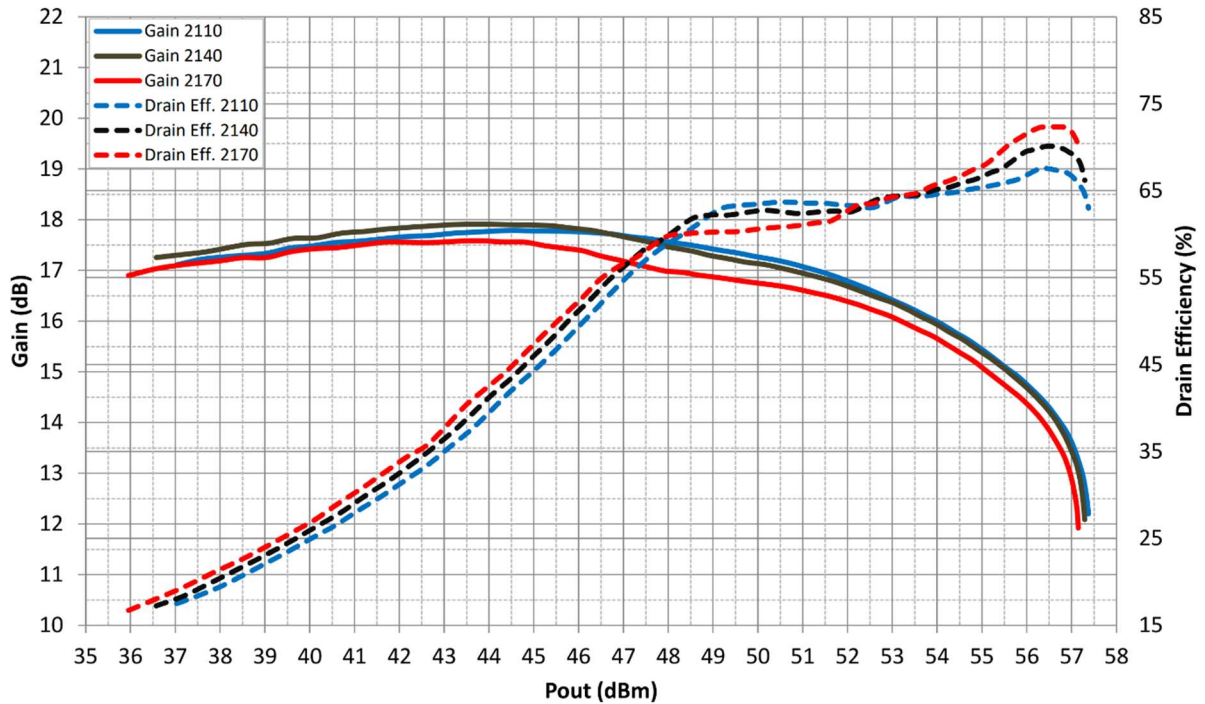


Figure 4: Network analyzer output, S11 and S21 (2.1-2.2GHz Doherty)

m1 freq=2.110 GHz dB(S(2,1))=18.401 dB(S(1,1))=-20.740	m2 freq=2.140 GHz dB(S(2,1))=18.567 dB(S(1,1))=-18.481	m3 freq=2.170 GHz dB(S(2,1))=18.379 dB(S(1,1))=-15.781
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S-Parameters_STBV22500BY4 DHT

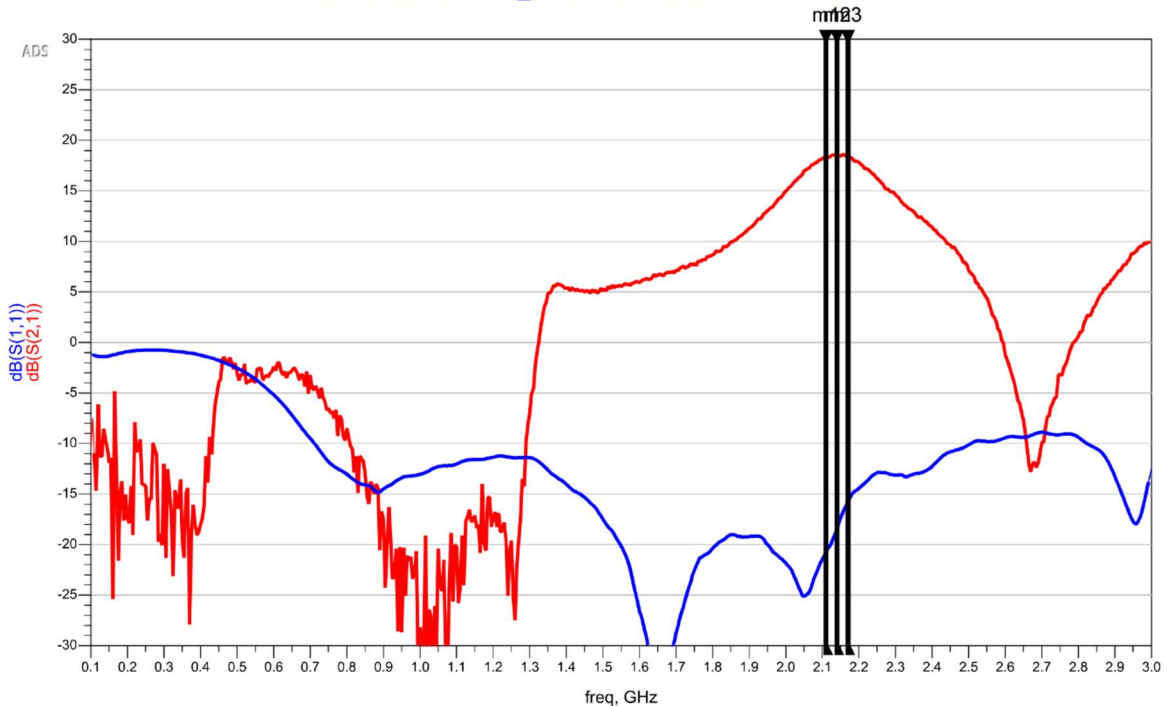


Figure 5: Picture of application board Doherty circuit for 2.1-2.2GHz

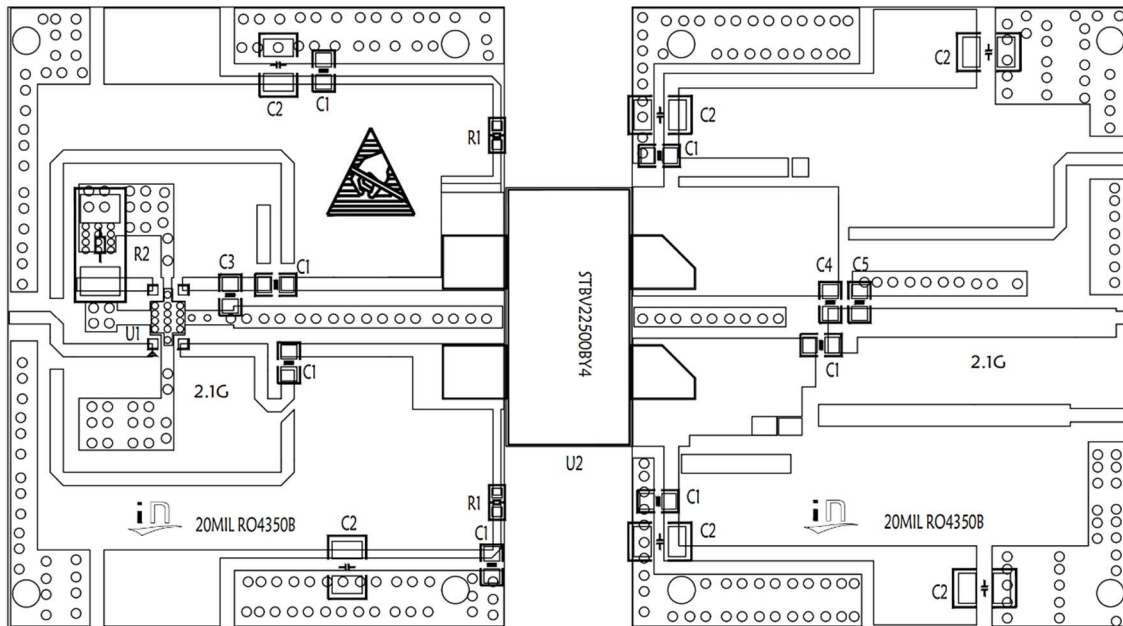
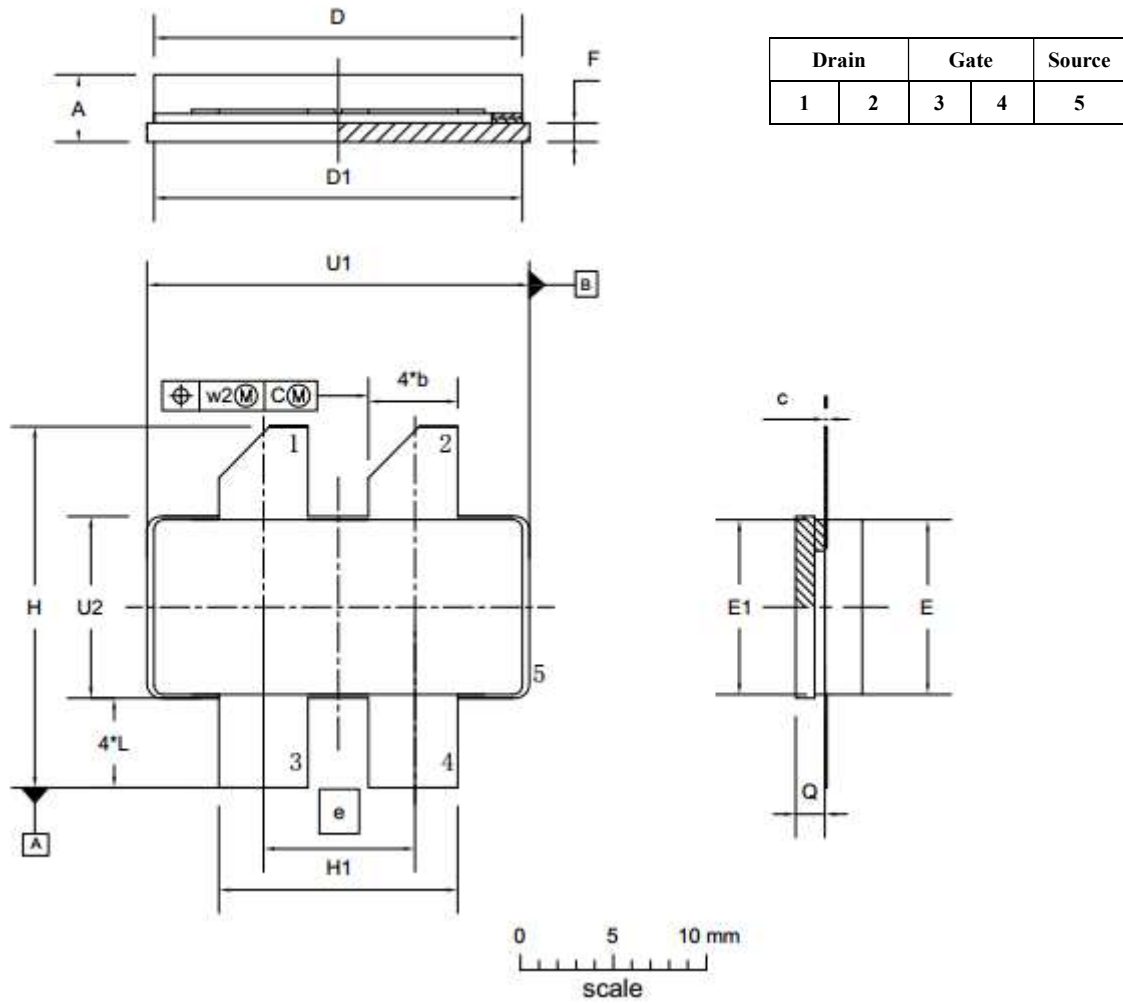


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1	0805	18pF/250V	7
C2	1210	10uF/100V	6
C3	0805	0.4pF/250V	1
C4	0805	2.2pF/250V	1
C5	0805	0.3pF/250V	1
R1	0603	10R	2
R2	2512	51R	1
U1	6.35*5.08mm	HC2100P03H	1
U2	BY4	STBV22500BY4	1



Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/6/1	V1.0	Preliminary Datasheet Creation
2021/8/25	V1.1	Add recommended driver
2022/5/17	V1.2	Modify the recommended band and driver
2022/9/30	V2.0	Modify according to configuration of main path and peak path

Application data based on: ZBB-22-11

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