



915MHz, 550W, 40V High Power RF LDMOS FETs

Description

The ITDE10550C2 is a 550-watt, internally matched LDMOS FET, designed for ISM applications including RF Energy at 915MHz. It can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal

In typical application using 2*ITDE10550C2 in parallel, it can deliver more than 850W CW with high efficiency



•Typical Performance using single **ITDE10550C2** (On Innegration fixture with device soldered):

VDD = 42Volts, I_{DQ} = 10 mA, CW signal

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
915	45.5	57.5	560	19.4	12	69%

Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Pb-free, RoHS-compliant
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	95	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+42	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _C = 85°C, T _J =200°C, DC test	R _{θJC}	0.25	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =100uA)	V _{DSS}	95	-----	-----	V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 40 V, V _{GS} = 0 V)	I _{DSS}	-----	-----	10	μA



Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 40\text{ V}$, $I_D = 600\text{ uA}$)	$V_{GS(th)}$	---	2.0	---	V
Gate Quiescent Voltage ($V_{DD} = 40\text{ V}$, $I_{DQ} = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.62	3.1	V

Functional Tests (On Innogrations Test Fixture, 50 ohm system) : $V_{DD} = 42\text{ Vdc}$, $I_{DQ} = 50\text{ mA}$, $f = 915\text{ MHz}$, $P_{in} = 45.5\text{ dBm}$ CW Signal Measurements.

Power Gain	G_p	---	12	---	dB
Drain Efficiency @ P_{OUT}	η_D	---	68	---	%
Output Power	P_{out}	---	550	---	W
Input Return Loss	IRL	---	-7	---	dB

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 42\text{ Vdc}$, $I_{DQ} = 10\text{ mA}$, $f = 915\text{ MHz}$

VSWR 10:1 at 550W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation
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**Reference Circuit of Test Fixture Assembly Diagram
1*ITDE10550C2**

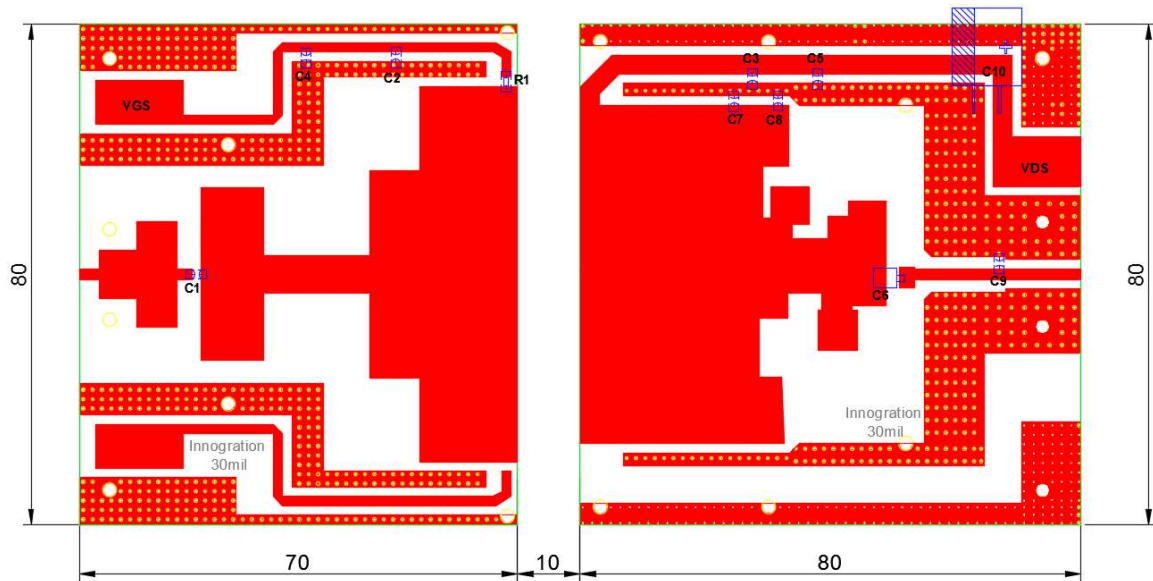


Figure 1. Test Circuit Component Layout

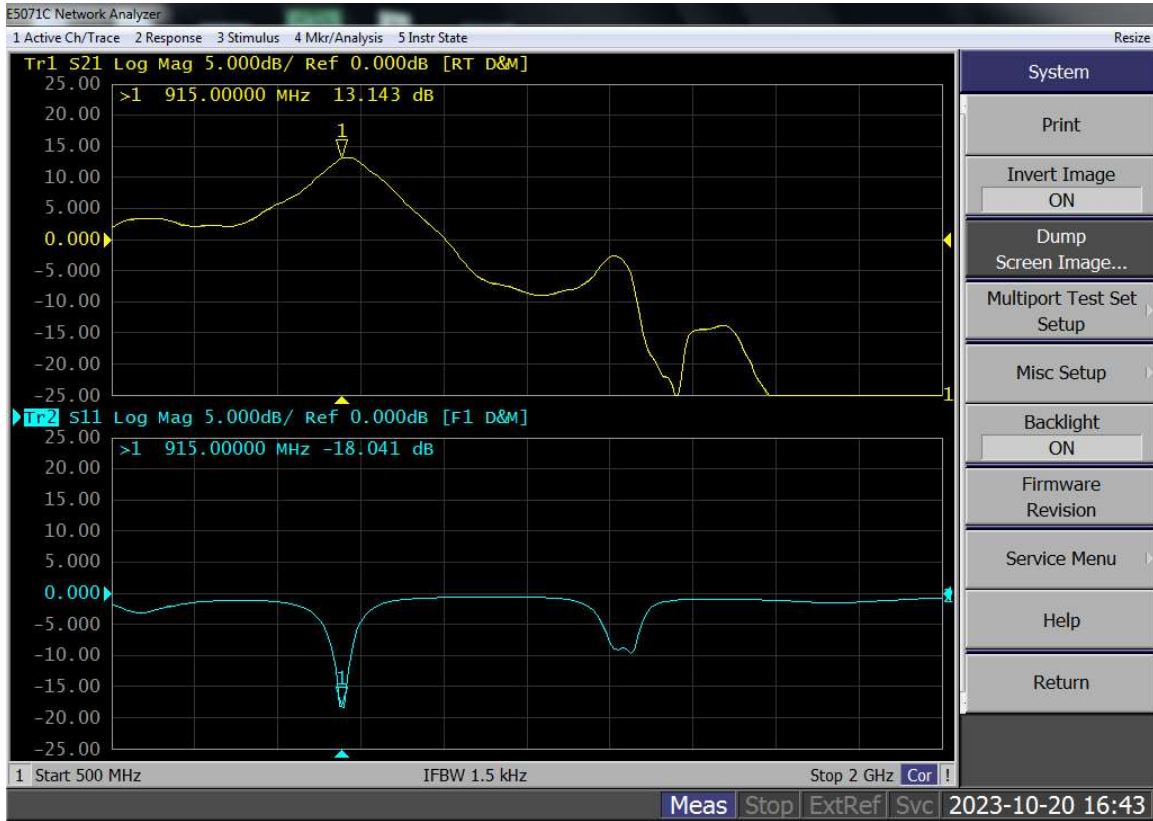
Table 1. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2,C3	75pF	MQ301111
C4,C5	10uF/100V	Ceramic multilayer capacitor
C6	100pF	MCM-1-300V-D-101J
C7,C8	1.2pF	MQ301111
C9	3.0pF	MQ301111
C10	4700uF/63V	Electrolytic Capacitor
R1	18 Ω	Chip Resistor
PCB	30mil Rogers 4350B	



CHARACTERISTICS

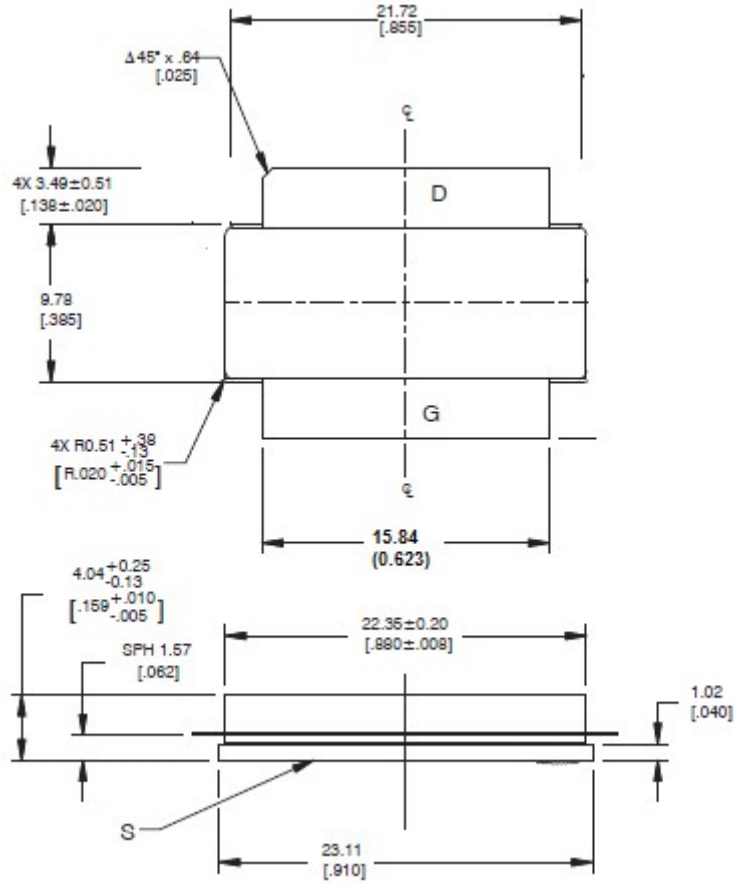
Figure 2. Network analyzer output S11/S21





Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/10/20	Rev 1.0	Preliminary Datasheet

Application data based on HL-23-50

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