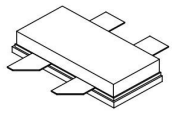
500W,50V RF LDMOS Transistor

ITEV10500B4



Description

The ITEV10500B4 is a 500watt capable, Doherty paired LDMOS transistor, ideal for for 4G/5G cellular applications from 0.6 to 1GHz..

It can be configured as asymmetrical Doherty delivering 80W average power, according to normal 8dB back off.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical Doherty RF Performance (On Innogration fixture with device soldered).

Vds=50V Idq_main=460mA, Vgs_peak=1.8V

Freq (MHz)	Pulse CW Signal			P_{avg}=49dBm WCDMA Signal		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	$ACPR_{5M}$ (dBc)
869	18.32	528.3	56.5	19	48.1	-28.7
881	18.28	538.7	58.3	19	48.2	-30.3
894	18.05	516.2	59.2	19	48.5	-32.6

Applications

- Asymmetrical Doherty amplifier within 0.6-1GHz
- UHF TV
- P band power amplifier

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

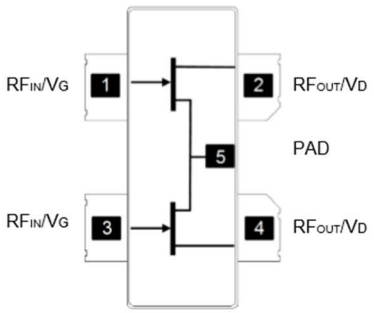


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 500mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 500mA, f = 894 MHz

VSWR 10:1 at 80W WCDMA Output Power	No Device Degradation

869-894MHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

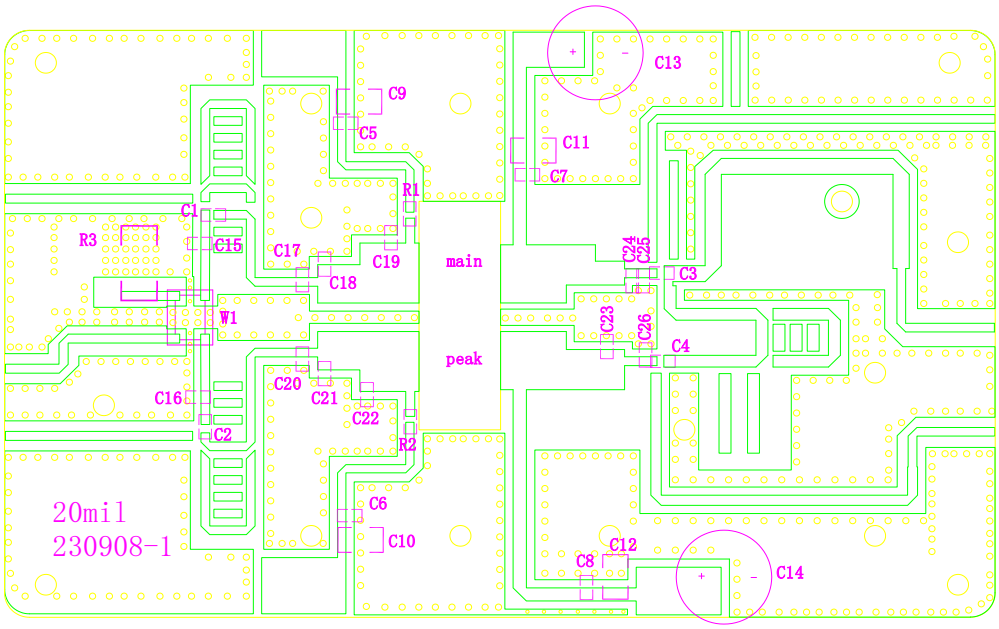


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C25, C26	0603	10 pF	4
C3, C17, C18, C19, C20, C21, C22, C23	0603	6.8 pF	8
C4, C5, C6, C7, C8	0603	68 pF	5
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		220uF/63V	2
C15	0603	2.7 pF	1
C16	0603	1.1 pF	1
C24	0603	2 pF	1
R1, R2	0603	10R	2
R3	2512	RFR50N-20CT0410B	1
W1		DC07F02（YANTEL 2dB)	1

(pF capacitors are ATC 600S series)

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=460mA

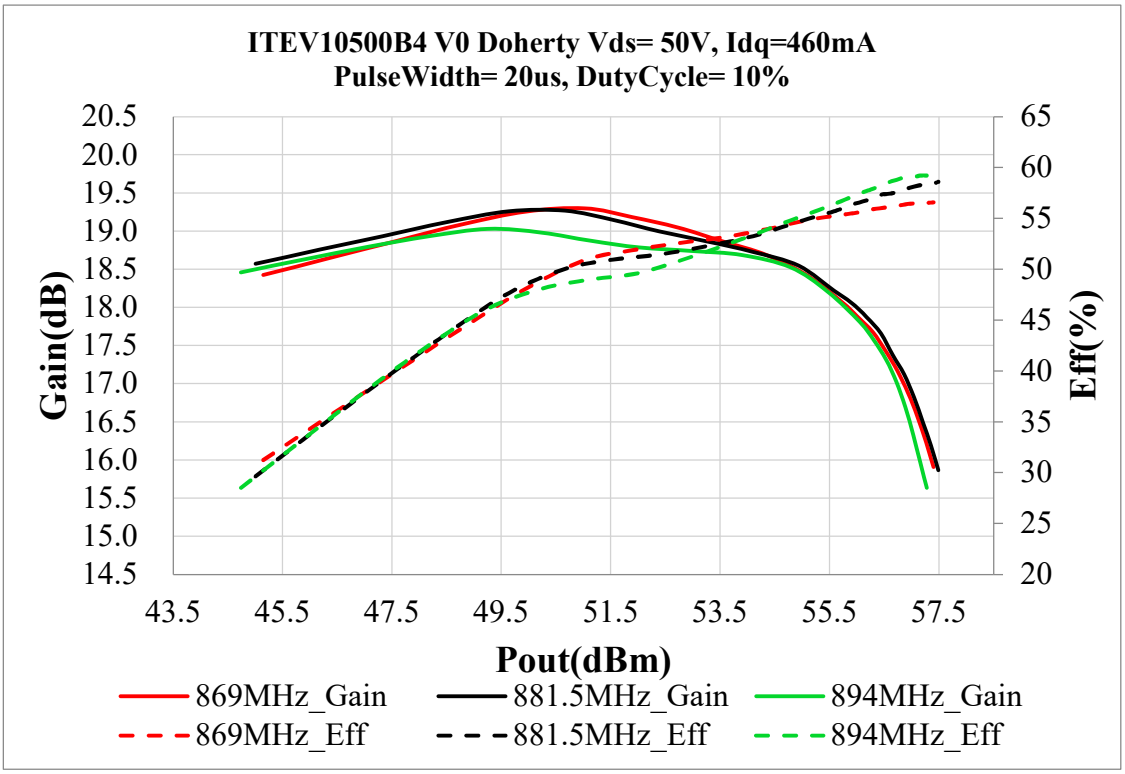
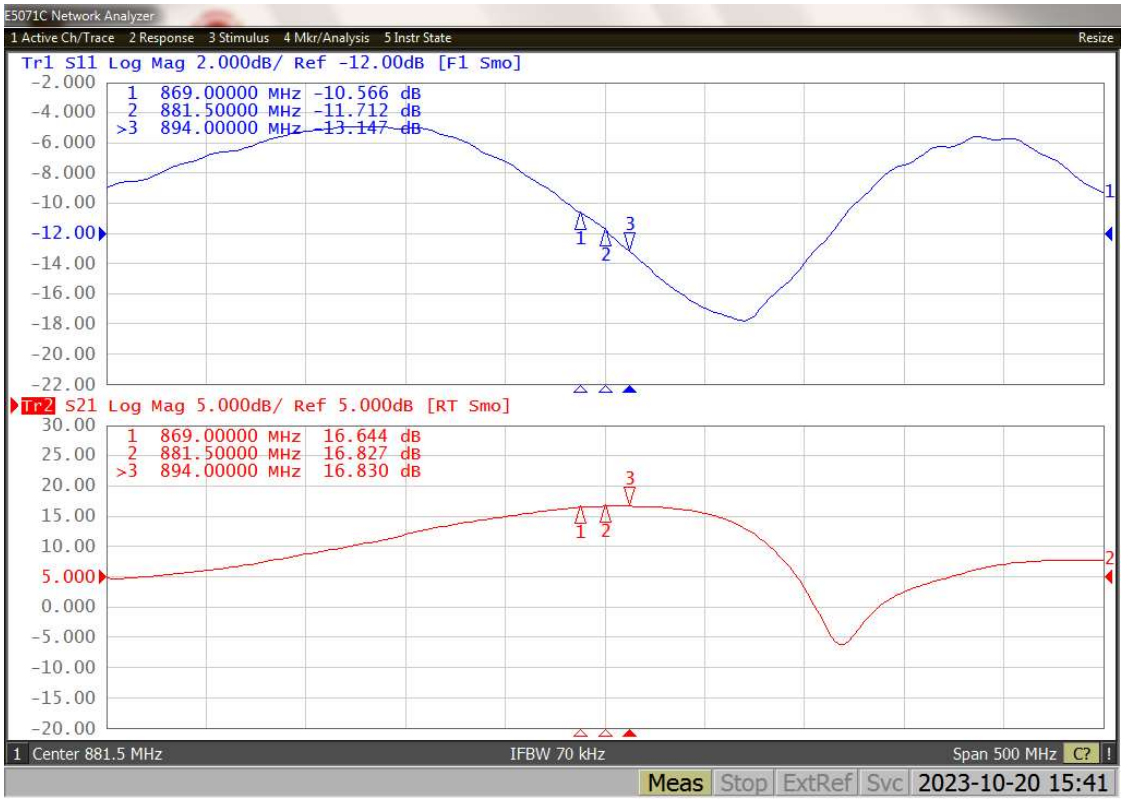
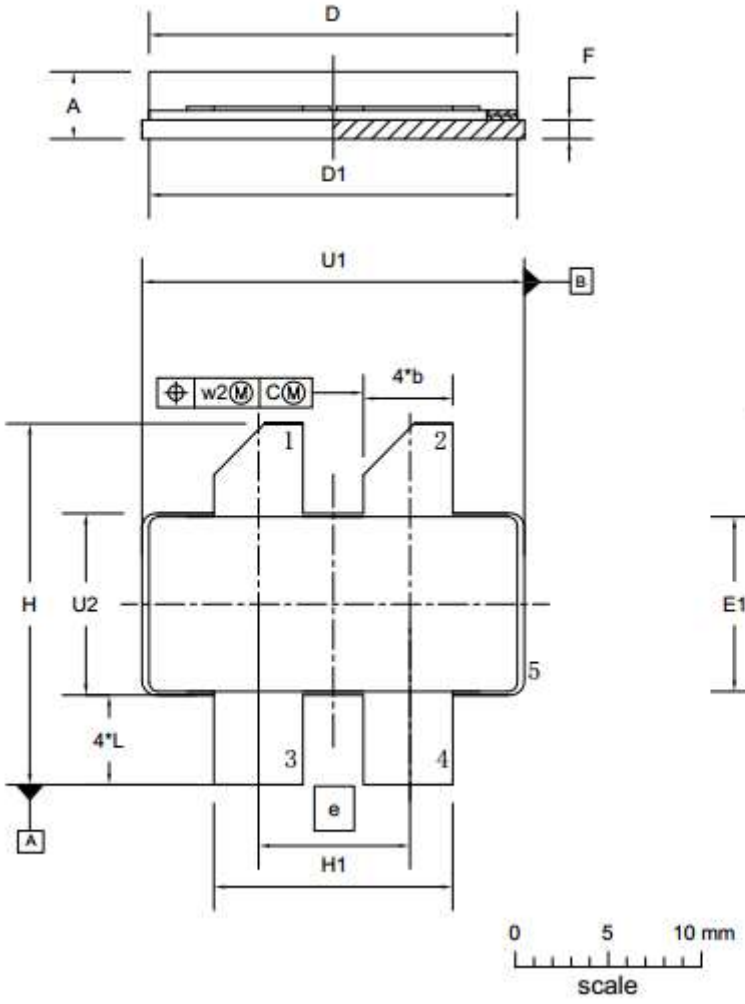


Figure 5.Network analyzer output S11/S21



Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/10/20	Rev 1.0	Preliminary Datasheet

Application data based on LSM-23-32

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