

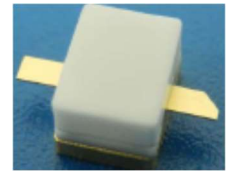


60W, 50V High Power RF LDMOS FETs

Description

The ITGV15060J2 is a 60-watt, LDMOS FET, designed for ISM applications up to 1.5GHz, including RF Energy at 915MHz/1300MHz etc. It can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal

ITGV15060J2



•Typical Performance at 915M/1300MHz (On Innegration fixture with device soldered):

Vds= 50V, Vgs=2.96V, Idq=10mA						
Freq(MHz)	Test signal	P-1(dBm)	P-1Gain(dB)	P-3(dBm)	P-3(W)	Eff (%)
915	Pulsed	47.66	21.1	48.57	71.9	65.0
	CW	47.42	20.8	48.16	65.4	62.1
1300	Pulsed	47.33	18.7	48.12	64.9	63.7
	CW	47.10	18.6	47.42	60.1	60.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	110	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+50	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, P _{out} =60W 915MHz	R _{θJC}	1.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =100uA)	V _{DSS}	106	---	---	V
Zero Gate Voltage Drain Leakage Current	I _{DSS}	---	---	10	μA



($V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$)					
Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{ V}$, $I_D = 600\text{ uA}$)	$V_{GS(th)}$	---	3	---	V
Gate Quiescent Voltage ($V_{DD} = 50\text{ V}$, $I_{DQ} = 10\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$		2.9		V

Functional Tests (On Innogrations Test Fixture, 50 ohm system) : $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 10\text{ mA}$, $f = 1.3\text{ GHz}$, $P_{in} = 32\text{ dBm}$ CW Signal Measurements.

Power Gain	G_p	---	16	---	dB
Drain Efficiency @ P_{OUT}	η_D	---	60	---	%
Output Power	P_{out}	---	60	---	W
Input Return Loss	IRL	---	-7	---	dB

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 10\text{ mA}$, $f = 1300\text{ MHz}$

VSWR 10:1 at 60W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

915MHz

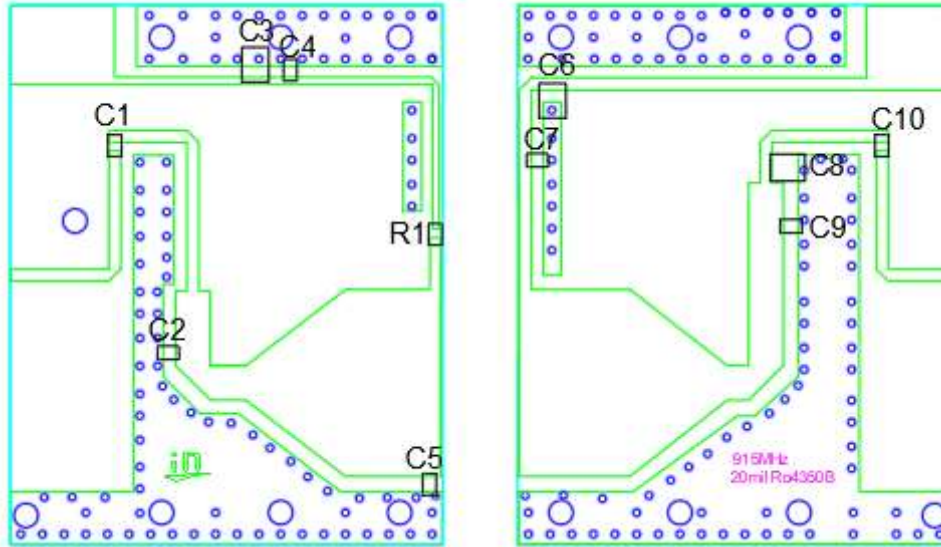


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Component	Value	Description
C1,C10	10pF	ATC600S
C2	8.2pF	ATC600S
C5	2.0pF	ATC600S
C3,C6	10uF	TDK1206
C4,C7	33pF	ATC600S
C8	5.1pF	ATC600S
C9	1.0pF	ATC600S
R1	10 Ω	

1300MHz

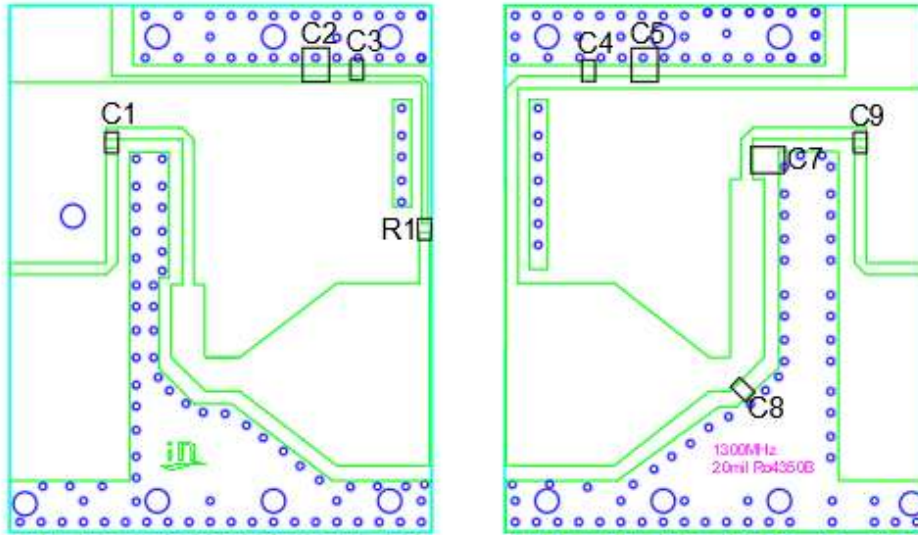


Figure 2 Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Component	Value	Description
C1,C9	10pF	ATC600S
C2,C5	10uF	TDK1206
C3,C4	33pF	ATC600S
C7	1.5pF	ATC600S
C8	7.5pF	ATC600S
R1	10 Ω	

Package Outline

Earless ceramic package; 2 leads

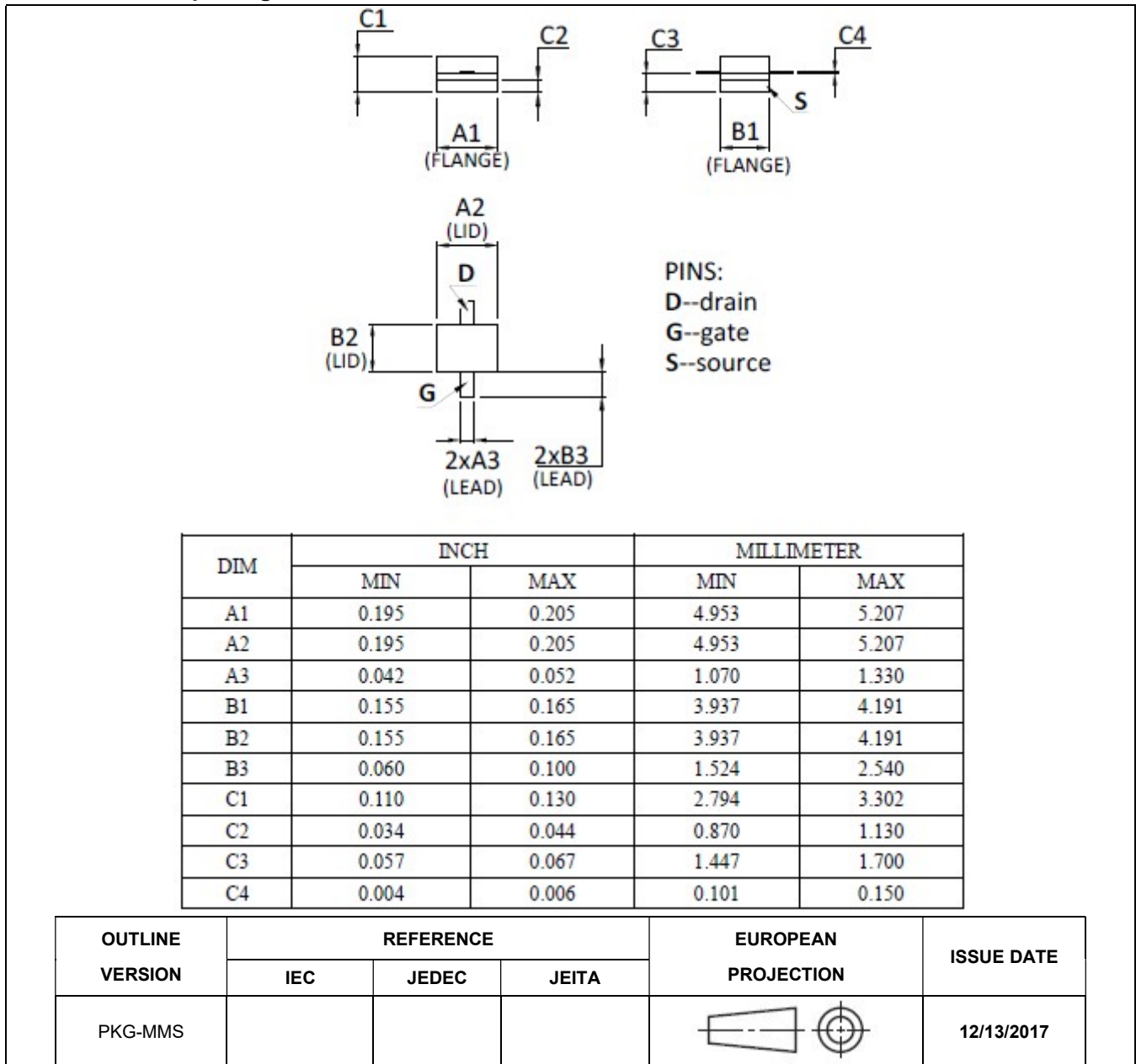


Figure 1. Package Outline PKG-MMS



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/10/23	Rev 1.0	Preliminary Datasheet

Application data based on HJ-23-18

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