

S3Q122K0RVP GaN TRANSISTOR

Document Number:
S3Q122K0RVP
Preliminary Datasheet V1.0

1030/1090MHz, 2000W, GaN RF Power Transistor

Description

The S3Q122K0RVP is a 2000-watt, high performance, internally matched GaN RF Power transistor, designed for multiple applications with frequencies 1030-1090MHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as Avionics application, L band pulse amplifier.

Please notice that both leads at input and output side are internally connected, to configure this device as single ended ,shown as right picture.



•Typical **Pulsed CW** Performance (On Innogration fixture with device soldered):

Vgs=-3.25V Vds=50V Idq=280mA ,Pulse 100us 10%								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff (%)	2 nd (dBc)	3 rd (dBc)
1030	63.17	2074.9	7.52	48.69	14.48	55.18	-29.10	-45.60

Applications and Features

- Suitable for L band pulse amplifier, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to 0	Vdc
Operating Voltage	V _{DD}	0 to 55	Vdc
Maximum forward gate current	I _{gf}	270	mA
Storage Temperature Range	T _{stg}	-65 to +150	C
Case Operating Temperature	T _c	-55 to +150	C
Operating Junction Temperature	T _j	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case 85 °C Case backside Temperature Pout = 2000 W, Pulse: 20 us PW, 10% DC	R _{θJC}	0.08	C/W

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Table 3. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}; I_{DS}=270\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 50\text{V}, I_D = 270\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}, I_{DS}=300\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system) : $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 300\text{mA}$, $f = 1030\text{MHz}$, Pulse CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ Psat	Gp		14		dB
Drain Efficiency@Psat	Eff		55		%
Saturated power	Psat		2000		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		Ψ

Reference Circuit of Test Fixture Assembly Diagram

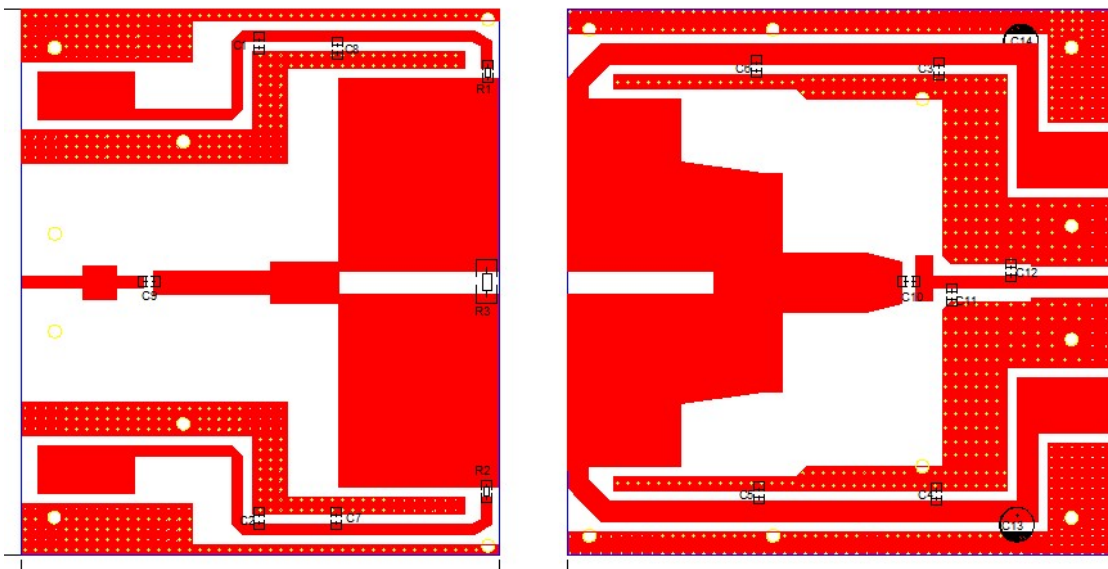


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1~C4	10uF	10uF/100V
C5~C8	82pF	MQ101111
C9	39pF	MQ101111
C10	39pF	MCM-1-300V-D-390J
C13,C14	4700uF/63V	Electrolytic Capacitor
C11,C12	1.5pF	MQ102525
R1,R2,R3	10 Ω	Chip Resistor
PCB	30mil Rogers4350	

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TYPICAL CHARACTERISTICS

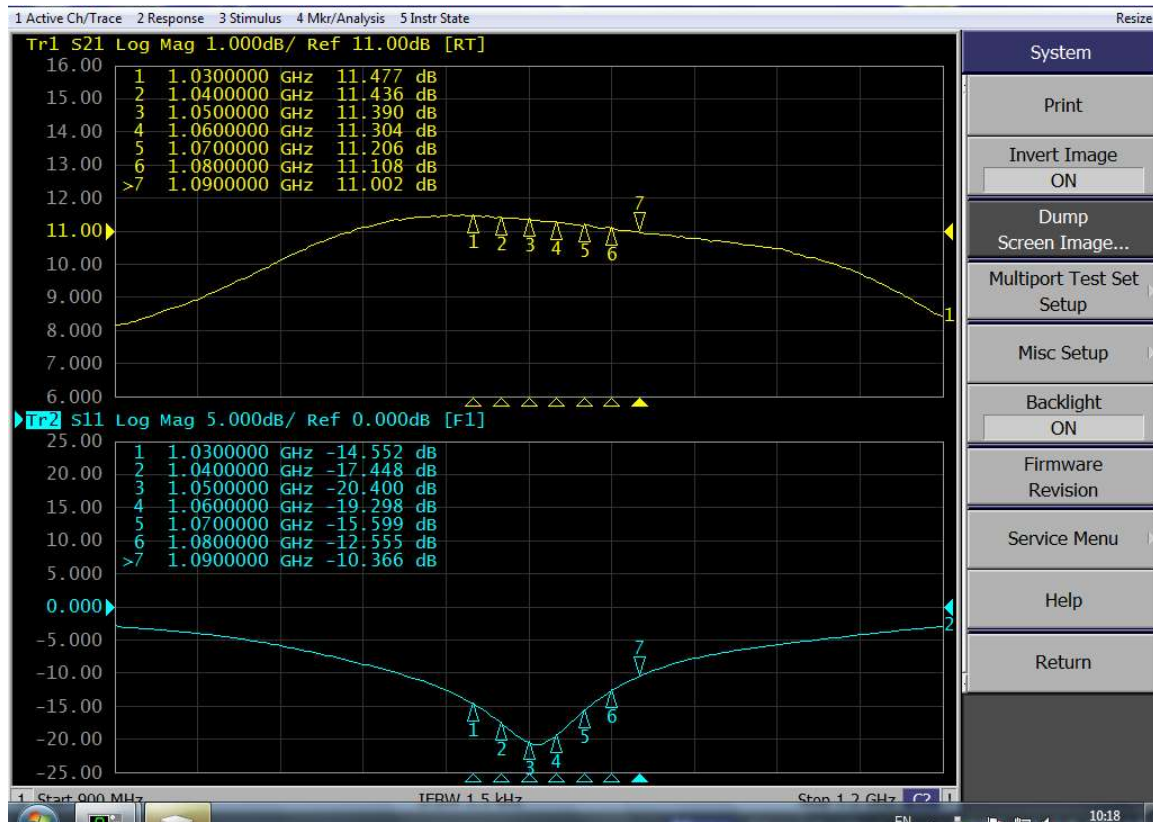


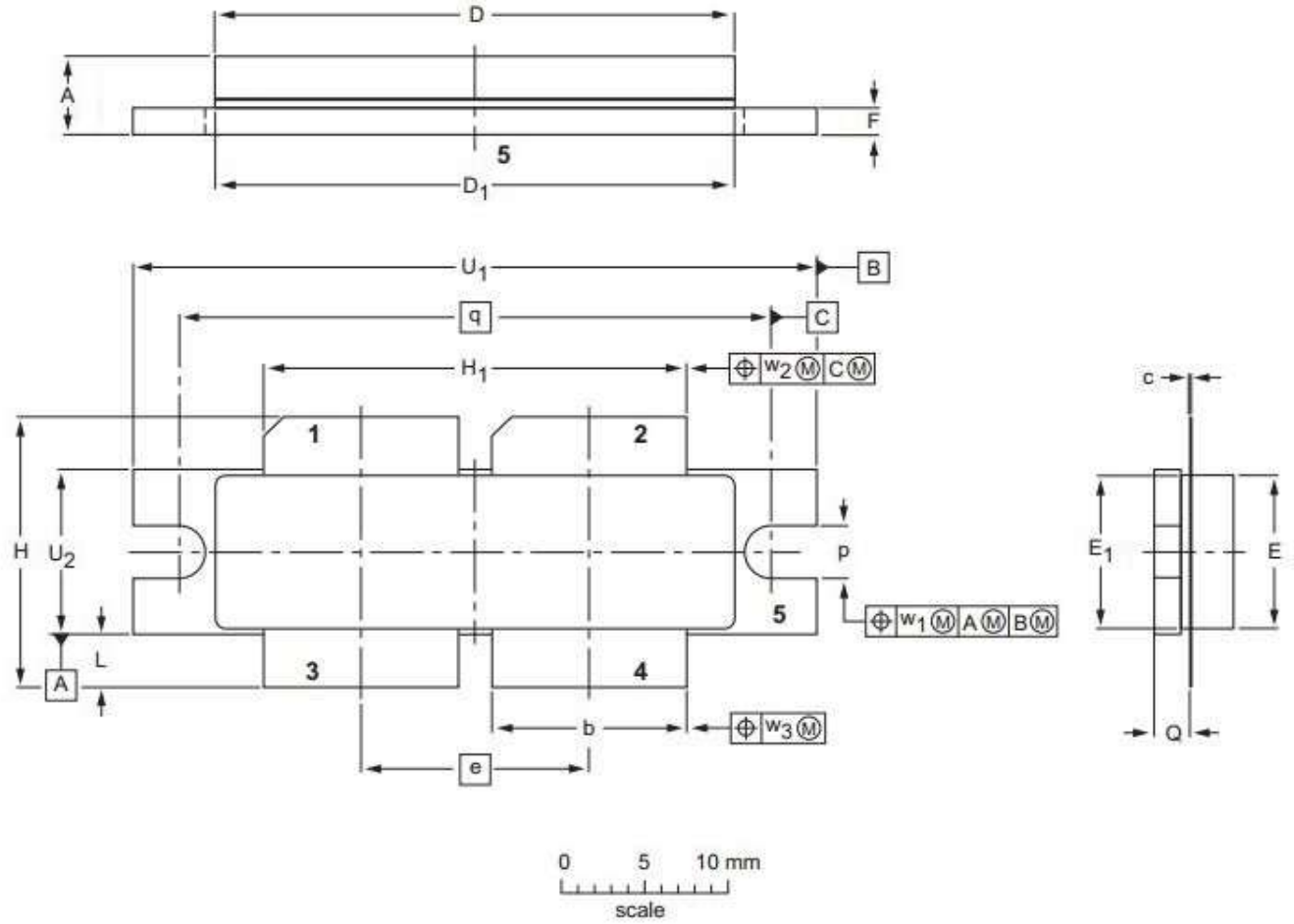
Figure 3. Network analyzer output S11/S21 at Idq=1A

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
Mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
Inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/11/14	Rev 1.0	Preliminary Datasheet

Application data based on TC-23-74

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