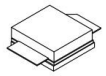
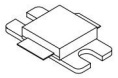
1800-2200MHz, 50W, 28V RF LDMOS FETs

ITCH22050A2



ITCH22050A2E



Description

The ITCH22050A2 is a 50-watt, internally-matched LDMOS FETs, designed for cellular and communication with frequencies from 1800 MHz to 2200 MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

•Typical Performance (On Test Fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 400 mA, Pulse CW, Pulse Width=20 us, Duty cycle=10%

Freq (GHz)	Pulse CW Signal(1)			P_{avg}=40.0dBm WCDMA Signal(2)		
	Gain_P1 (dB)	P3dB (dBm)	P3dB (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
1.98	18.02	48.51	71.0	19.26	27.56	-34.11
1.995	17.84	48.38	68.8	19.47	27.93	-33.08
2.01	18.55	48.23	66.6	19.62	28.35	-33.61

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	-55~+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 87°C, T_J=175°C, DC test	$R_{\theta JC}$	1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA

Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		2.0		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 400 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.8		V

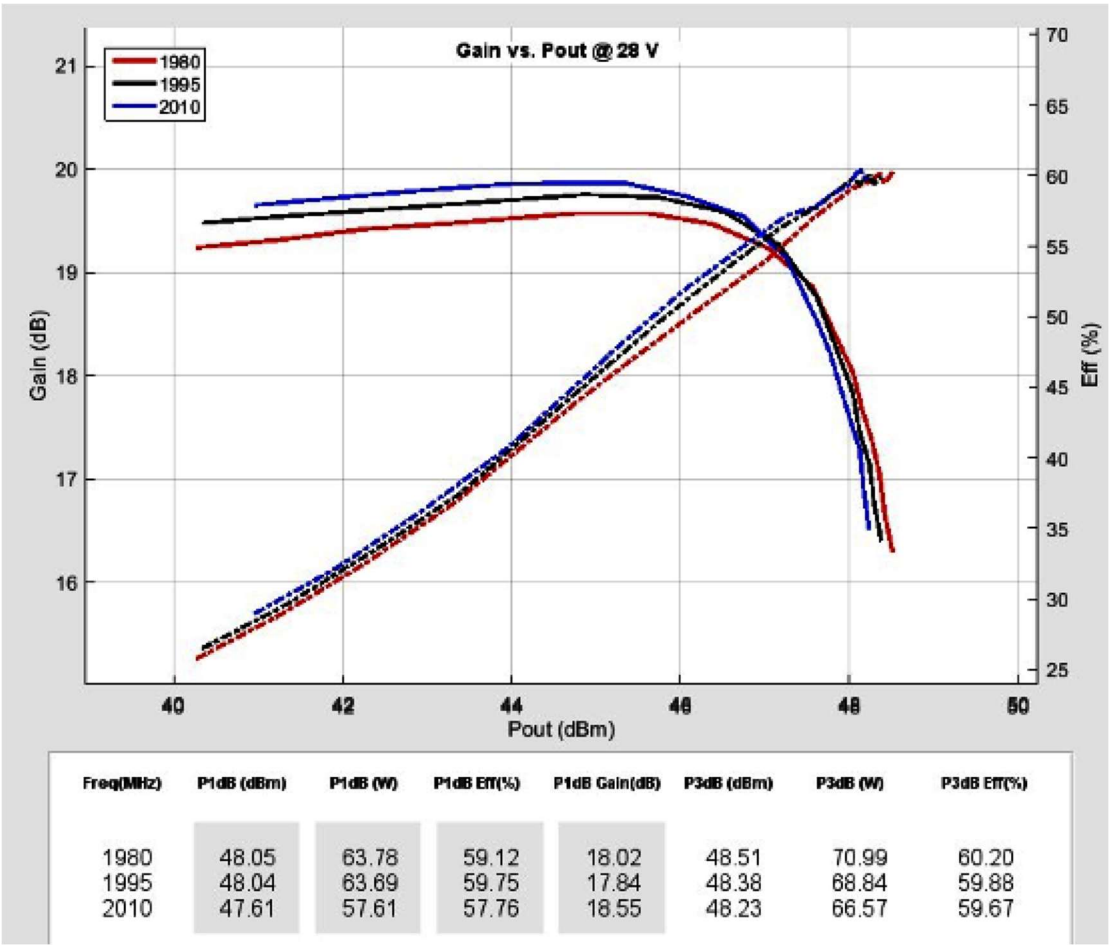
Functional Tests (In Innogration Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 400 mA, f =2000 MHz, CW Signal Measurements.

Power Gain @ P_{1dB}	Gp		18		dB
1 dB Compression Point	P_{-1dB}		47		W
Drain Efficiency@P_{1dB}	η_D		55		%
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 400 mA, f = 2000 MHz

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1980	48.05	63.78	59.12	18.02	48.51	70.99	60.20
1995	48.04	63.69	59.75	17.84	48.38	68.84	59.88
2010	47.61	57.61	57.76	18.55	48.23	66.57	59.67

Figure 2. Power Gain and Drain Efficiency as function of Power Out

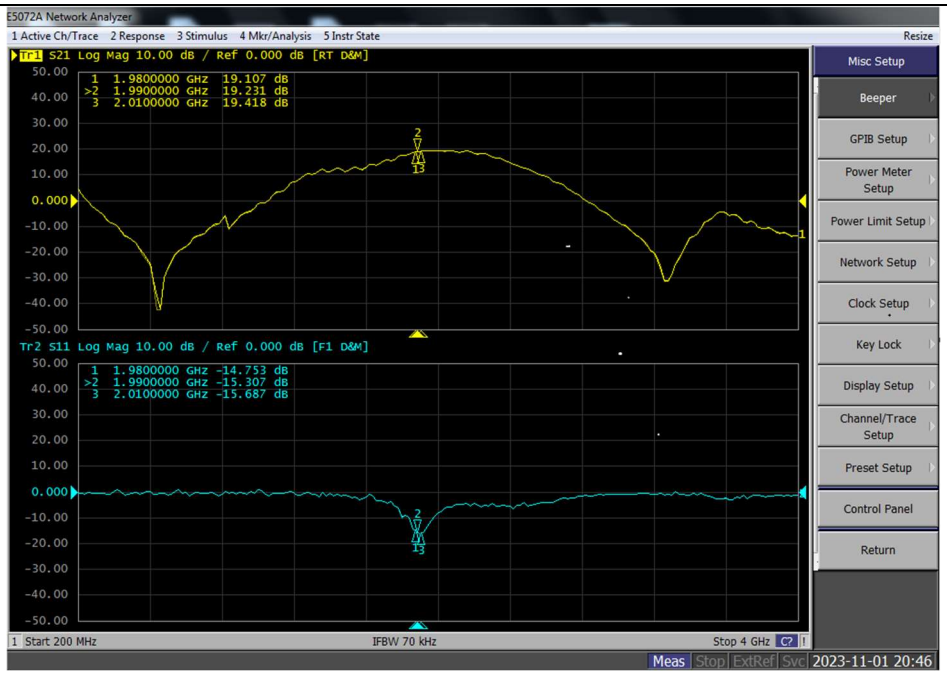


Figure 3. S11 and S21 of Network analyzer output

Reference Circuit of Test Fixture Assembly Diagram

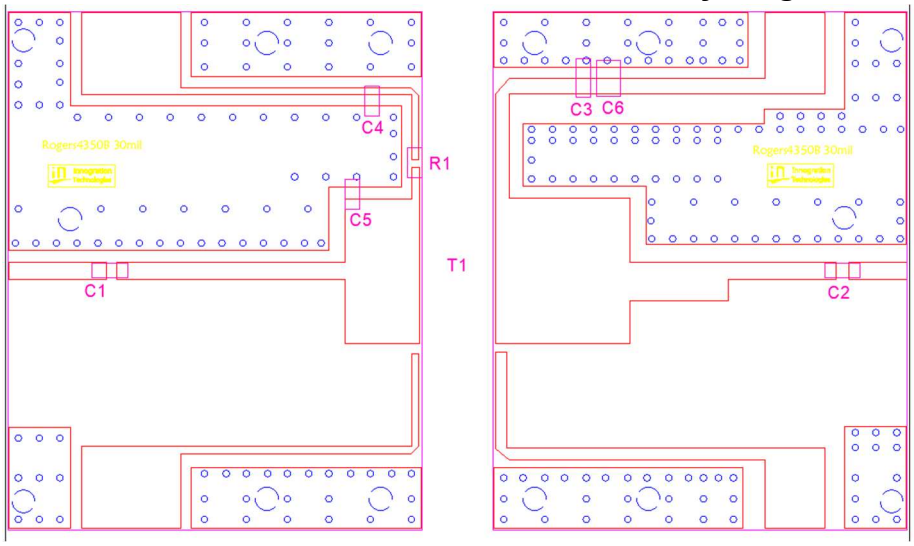
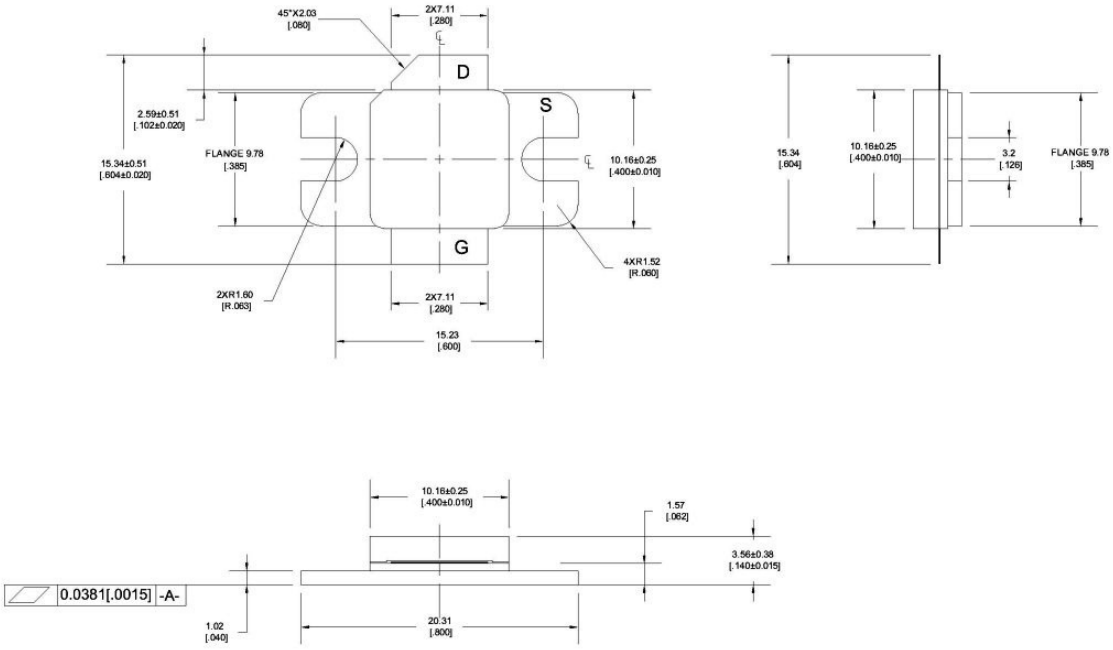


Table 5. Test Circuit Component Designations and Values

Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3,C4	4	20pF High Q Capacitor	251SHS200BSE	TEMEX
C5	1	1.5pF High Q Capacitor	251SHS1R5BSE	TEMEX
C6	1	10uF MLCC	GRM32EC72A106ME05	Murata
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	50W LDMOS Transistor	ITCH22050A2E	Innogration

Package Outline

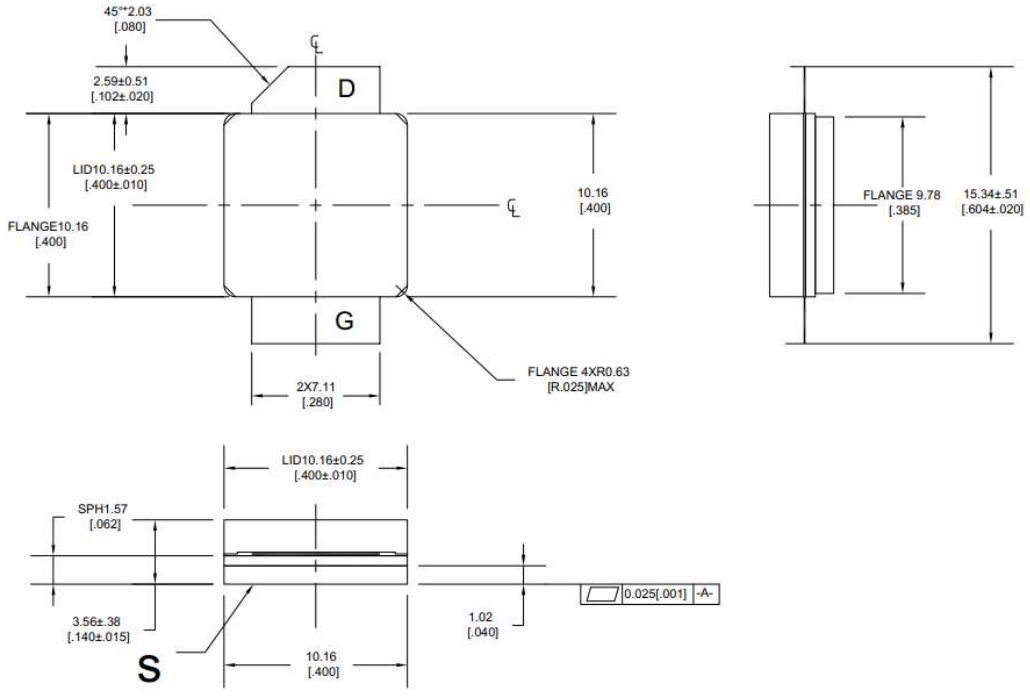
Eared Flanged ceramic package; 2 leads (A2E)



Unit：mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Earless Flanged ceramic package; 2 leads (A2)



Unit： mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/11/2	Rev 1.0	Product Datasheet

Application data based on LWH-23-20

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