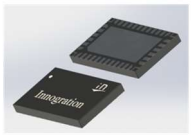
Gallium Nitride 50V, 90W, 3.3-4GHz RF Power Transistor

STAV40090C6



Description

The STAV40050BY4V is a 90-watt, internally matched GaN HEMT, designed for 5G cellular applications with frequencies from 3.3-4GHz.It can be configured as asymmetrical Doherty for 4G or 5G application, delivering 14W average power, according to normal 8 dB back off. There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

V_{DD} = 50 Vdc, I_{DQA} = 60 mA, V_{GSB} = –5.5Vdc,

Freq (GHz)	Pulse CW Signal(1)			P_{avg}=41.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	Psat (dBm)	Psat (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
3.7	14.05	49.67	92.65	13.68	54.75	-29.93
3.85	15.34	49.56	90.29	14.29	56.07	-29.60
4.0	14.15	49.41	87.24	13.22	53.05	-32.86

- Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

V_{DD} = 50 Vdc, I_{DQA} = 60 mA, V_{GSB} = –5.5Vdc,

Freq (GHz)	Pulse CW Signal(1)			P_{avg}=41.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	Psat (dBm)	Psat (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
3.4	13.54	50.05	101.18	13.27	53.58	-28.44
3.6	15.24	49.69	93.19	13.74	54.33	-30.60
3.8	14.68	49.73	94.05	13.03	53.85	-29.31

- Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

V_{DD} = 50 Vdc, I_{DQA} = 60 mA, V_{GSB} = –5.5Vdc,

Freq (GHz)	Pulse CW Signal(1)			P_{avg}=41.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	Psat (dBm)	Psat (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
3.3	15.41	49.79	95.32	15.29	55.20	-27.15
3.45	16.07	49.86	96.92	15.83	54.40	-29.44
3.6	16.60	49.64	92.04	16.10	54.38	-30.35

(1)Pulsed condition: 20us and 10%,

(2)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Applications

- 5G, 4G wireless infrastructure
- Wideband or narrowband power amplifier
- Test instruments
- S band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

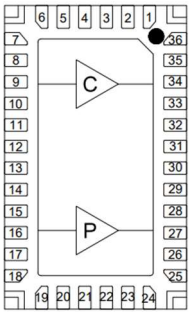
1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9	RF IN/Vgs1	RF Input, Vgs bias for carrier path
15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
1	VDD1	VDD bias for Carrier path
24	VDD2	VDD bias for Peak path
34,35	RF Out 1	RF Output for main path
27,28	RF Out 2	RF Output for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	11.5	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, Pdiss=9W at Pavg=41.5dBm WCDMA 1 carrier	$R_{\theta JC}$	3	°C /W

Notes: Based on expected carrier amplifier efficiency of Doherty, Pavg assumes 10% peaking amplifier contribution of total average Doherty

rated power. Thermal resistance is measured to package backside

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=4mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 4mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=60mA, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=7.5mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 7.5mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=60mA, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	3.8GHz, Pout=41.5dBm WCDMA 1 Carrier, All phase, No device damages	VSWR		10:1		

3.7-4.0GHz Doherty Application

Figure 2: Efficiency and power gain as function of Pout (Measured on 3.7-4.0GHz Doherty board)

V_{DD} = 50 Vdc, I_{DQ} = 60mA, Pulse width=50us, duty cycle=20%

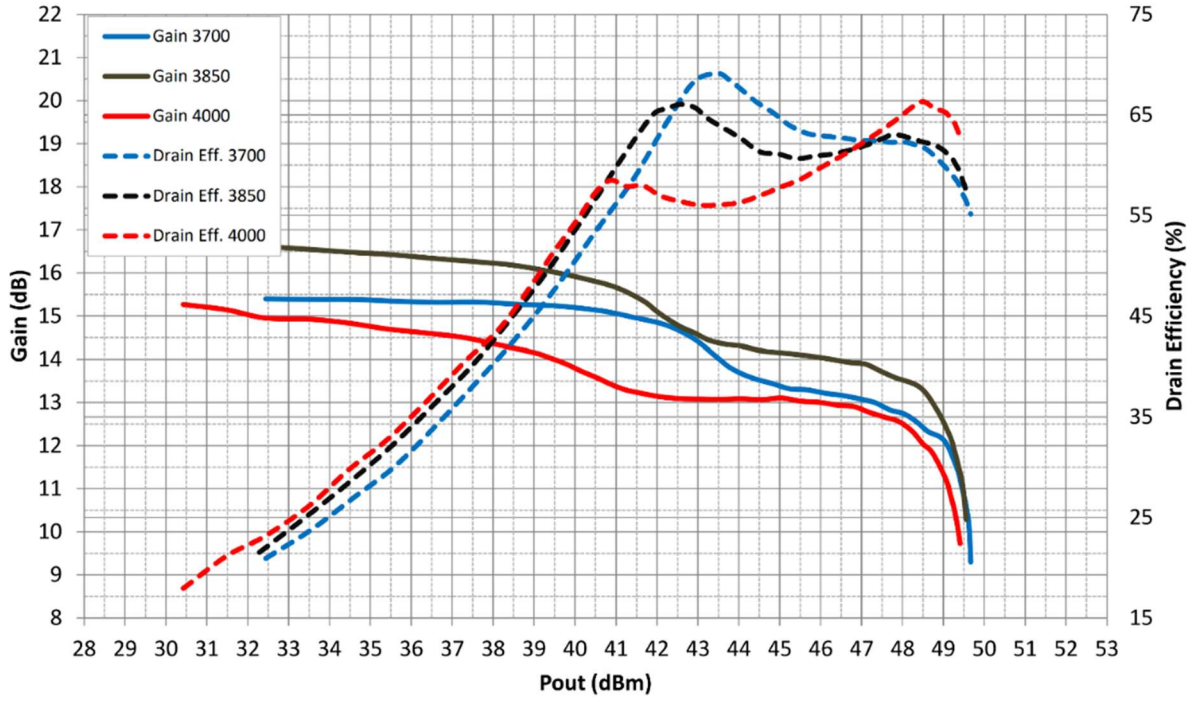


Figure 3: Network plot for S11/S21

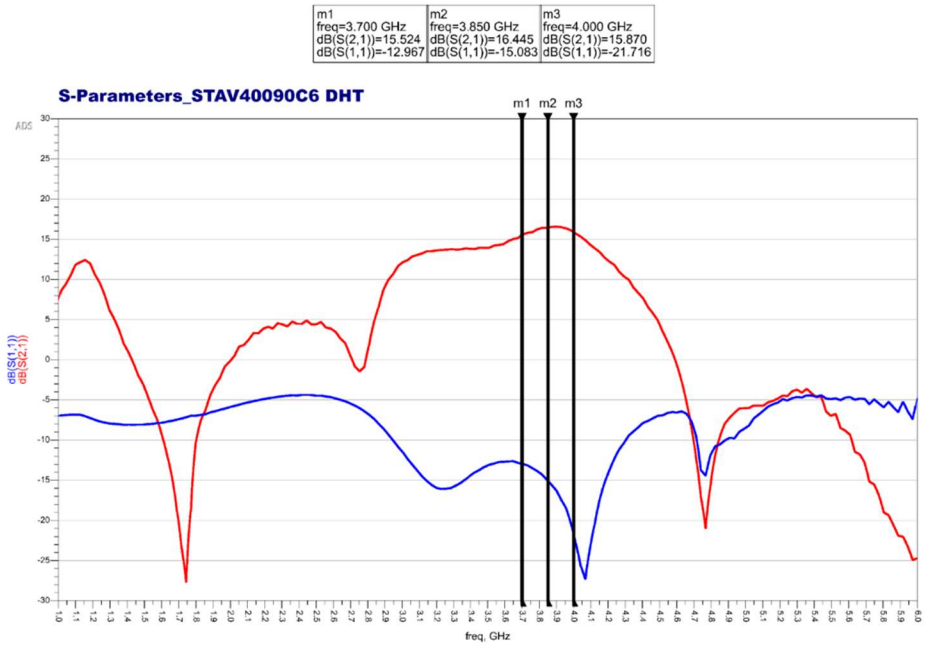


Figure 4: Picture of application board of 3.7-4.0GHz Doherty

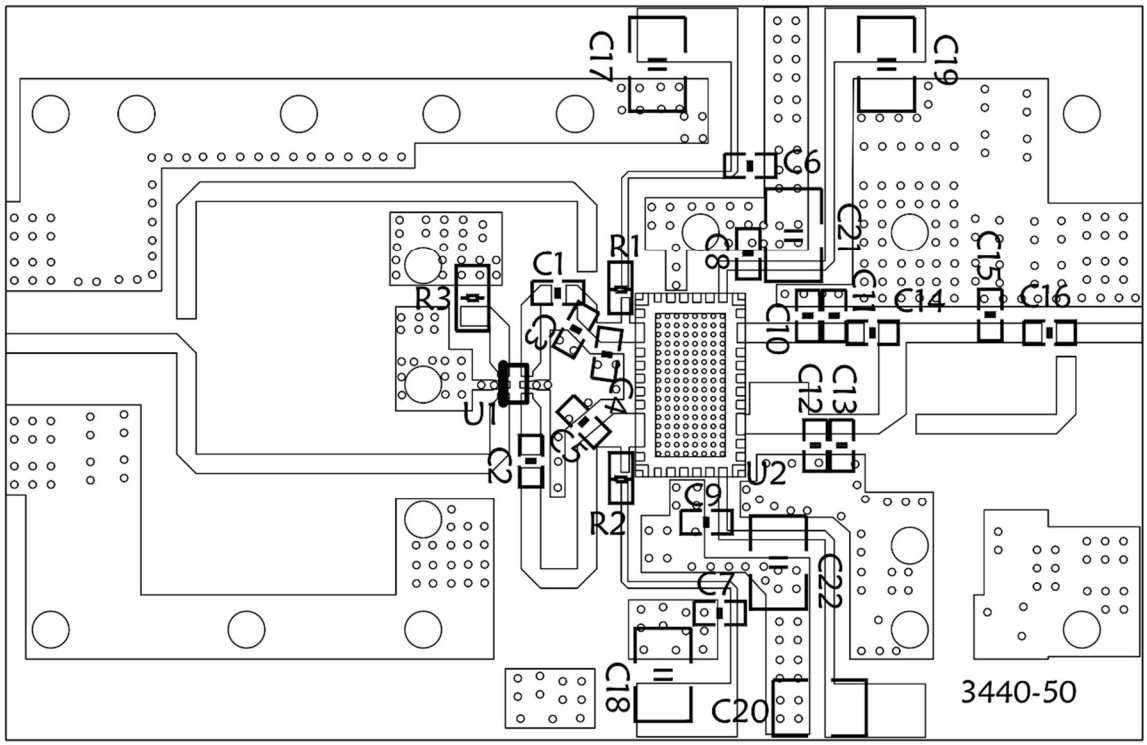


Table 4. Bill of materials of application board (RO4350B 20mils, PCB layout upon request)

Reference	Footprint	Value	Quantity
C1, C2, C6, C7, C8, C16	0603	8.2pF/250V	6
C3, C4	0603	0.9pF/250V	2
C5	0603	0.7pF/250V	1
C9	0603	3.0pF/250V	1

C10	0603	0.5pF/250V	1
C11, C12	0603	0.3pF/250V	2
C13	0603	0.6pF/250V	1
C14	0603	1.6pF/250V	1
C15	0603	0.5pF/250V	1
C17, C18, C19, C20, C21, C22	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	0805	50R	1
U1	0805	C3337J5003AHF	1
U2	C6	STAV40090C6	1

3.4-3.8GHz Doherty Application

Figure 5: Efficiency and power gain as function of Pout (Measured on 3.4-3.8GHz Doherty board)

V_{DD} = 50 Vdc, I_{DQ} = 60mA, Pulse width=50us, duty cycle=20%

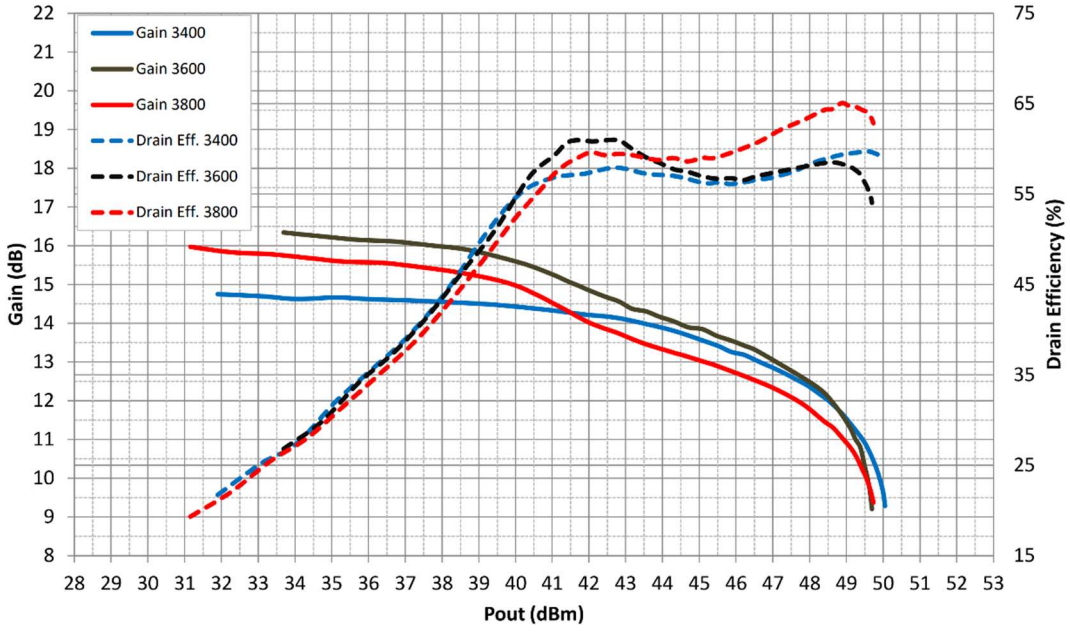


Figure 6: Network plot for S11/S21

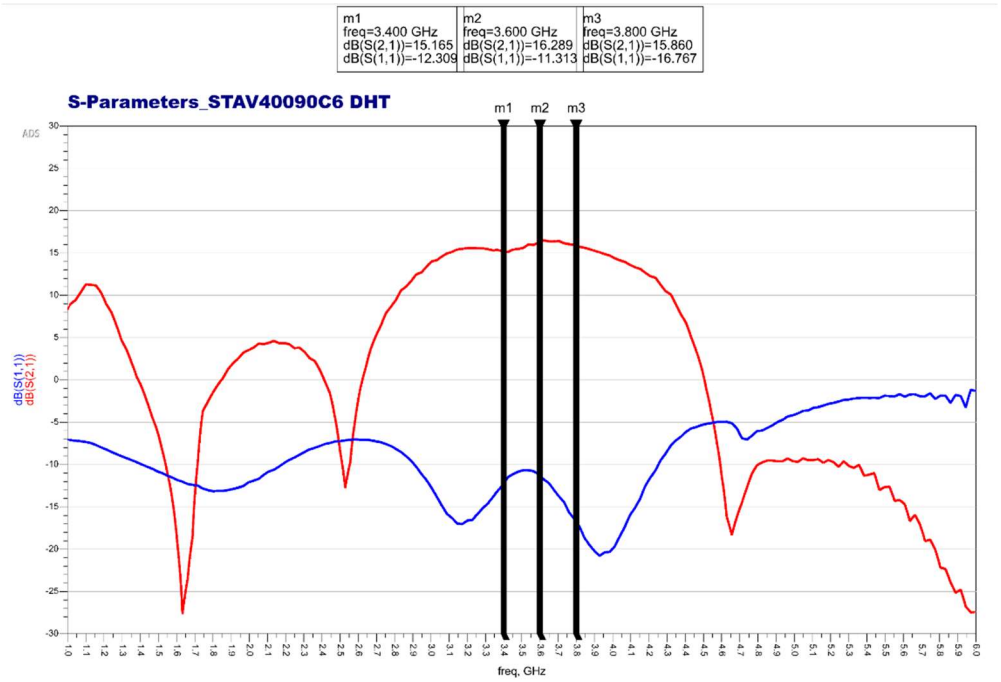


Figure 7: Picture of application board of 3.4-3.8GHz Doherty

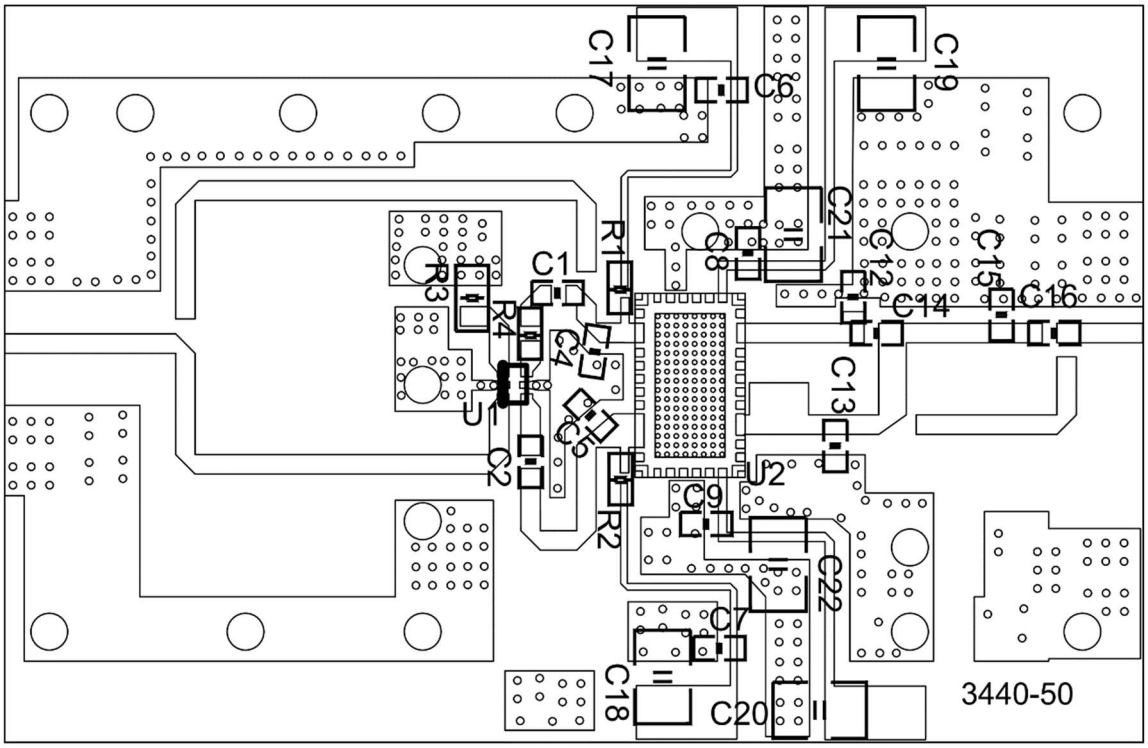


Table 4. Bill of materials of application board (RO4350B 20mils, PCB layout upon request)

Reference	Footprint	Value	Quantity
C1, C2, C6, C7, C8, C16	0603	8.2pF/250V	6
C4	0603	1.1pF/250V	1
C5	0603	1.3pF/250V	1
C9	0603	3.9pF/250V	1
C12	0603	0.5pF/250V	1
C13	0603	0.6pF/250V	1
C14	0603	1.8pF/250V	1
C15	0603	0.5pF/250V	1
C17, C18, C19, C20, C21, C22	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	0805	50R	1
R4	0805	9.1R	1
U1	0805	C3337J5003AHF	1
U2	C6	STAV40090C6[v1]	1

3.3-3.6GHz Doherty Application

Figure 8: Efficiency and power gain as function of Pout (Measured on 3.3-3.6GHz Doherty board)

V_{DD} = 50 Vdc, I_{DQ} = 60mA, Pulse width=50us, duty cycle=20%

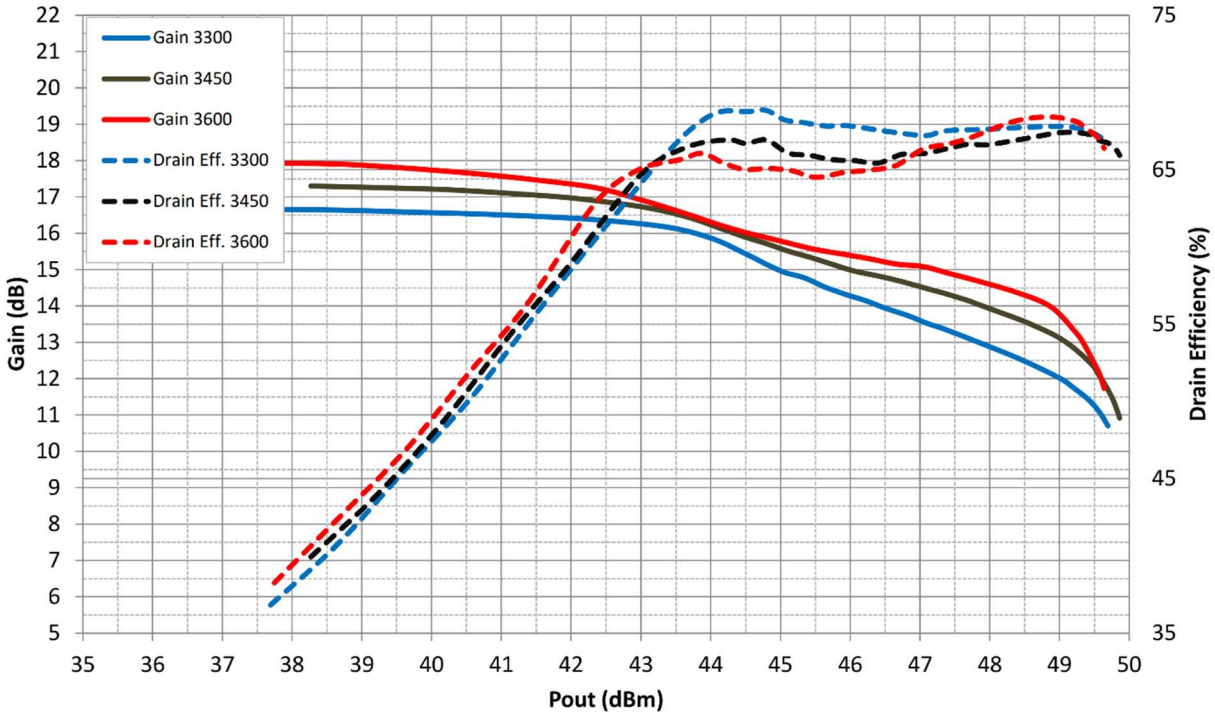


Figure 9: Network plot for S11/S21

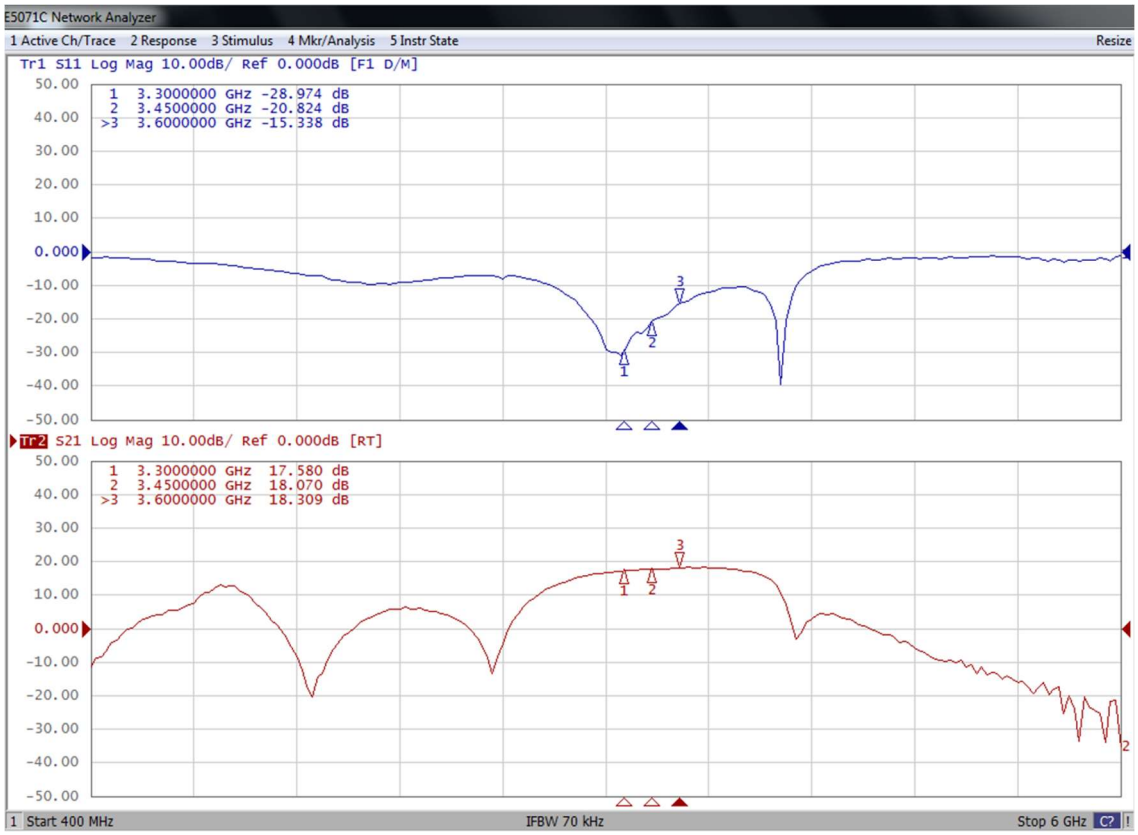


Figure 10: Picture of application board of 3.3-3.6GHz Doherty

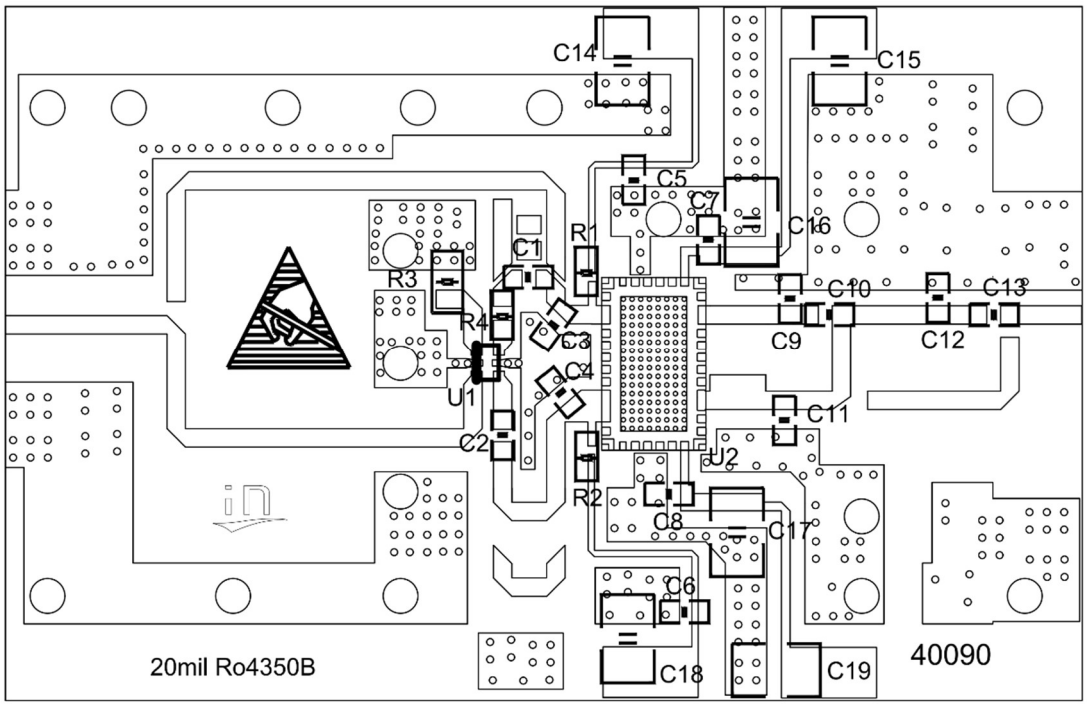


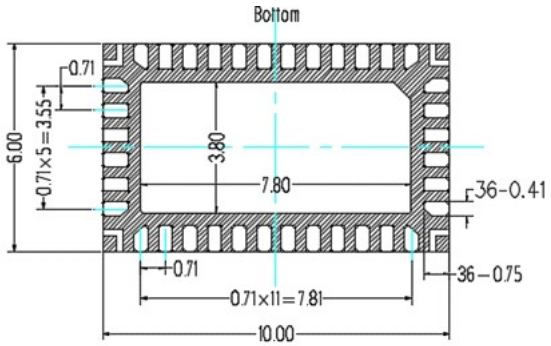
Table 5. Bill of materials of application board (RO4350B 20mils, PCB layout upon request)

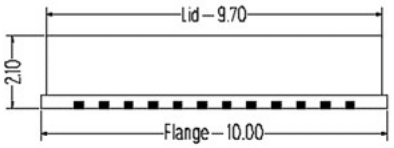
Reference	Footprint	Value	Quantity
C1, C2, C5, C6, C7, C13	0603	8.2pF/250V	6

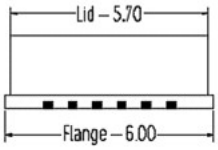
C3	0603	1.2pF/250V	1
C4	0603	1.3pF/250V	1
C9	0603	0.7pF/250V	1
C10	0603	1.8pF/250V	1
C12	0603	0.5pF/250V	1
C11	0603	1.0pF/250V	1
C8	0603	3.9pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	0805	50R	1
R4	0805	0R	1
U1	0805	C3337J5003AHF	1
U2	C6	STAV40090C6	1

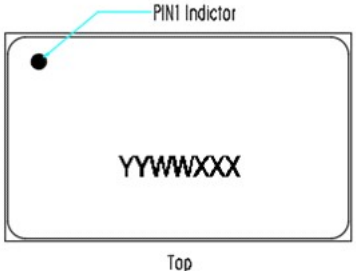
Package Dimensions

10*6 Plastic Package









Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/12/7	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: ZBB-23-34/35/37

Notice