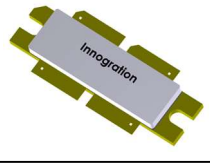
MQ011K3VPX LDMOS TRANSISTOR

Document Number: MQ011K3VPX
Preliminary Datasheet V1.0

1300W, 50V High Power RF LDMOS FETs

MQ011K3VPX



Description

The MQ011K3VPX is a 1300-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 150MHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV applications.

- Typical Performance (On Innogration fixtures with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 100 mA, CW

Freq(MHz)	Pin（W）	Pout(W)	Gain(dB)	Eff(%)
13.56	18	1400	18.5	80
85	20	1300	18	80
100	25	1300	17	79

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	140	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 1300W CW, 50 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$	0.11	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.03	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics (Per Side)

Drain-Source Voltage V_{GS}=0, I_{DS}=18.0mA	$V_{(BR)DSS}$		140		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.2		V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		620		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		130		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		2.8		pF

Reference Circuit of Test Fixture (88-108MHz)

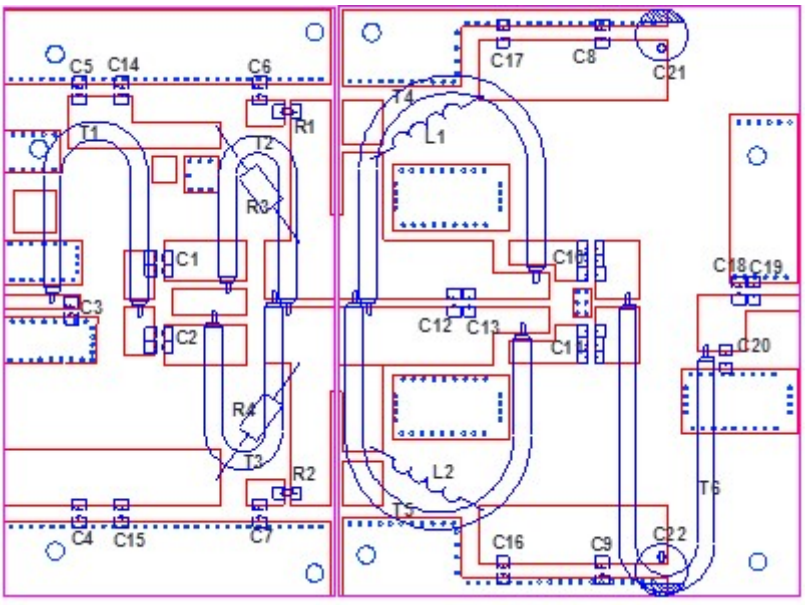


Figure 1. Test Circuit Component Layout

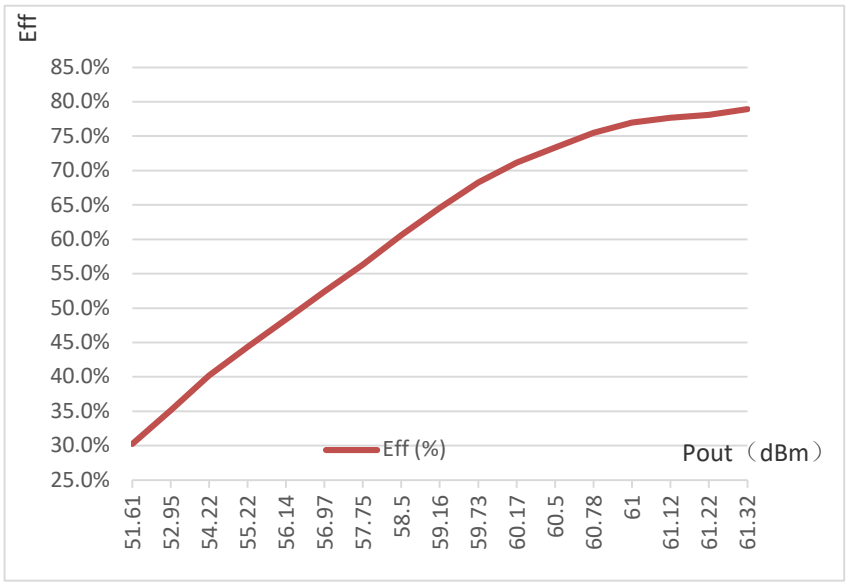
Part	description	Model
C1, C2, C6, C7, C10, C11, C16, C17	470PF	DLC70B
C3	1.5PF	DLC75D
C4, C5, C6, C7, C8, C9	10UF	100V/10UF
C10,C11	470PF*3	DLC70B

C12	4.7PF	DLC70B
C13	10PF	MIN02-002CC100J-F
C14~C17	1000PF	DLC70B
C18	2.2PF	DLC70B
C19,C20	3.3PF	DLC70B
R1,R2	39Ω*2	0805
R3,R4	470Ω	1W/470Ω
L1, L2	50nH	DIY
T1	50Ω,150mm	SF-086-50
T2,T3	25Ω,150mm	SFF-25-1.5
T4,T5	12.5Ω,170mm	SFF-12.5-1.5
T6	50Ω,200mm	RG402-3

TYPICAL CHARACTERISTICS

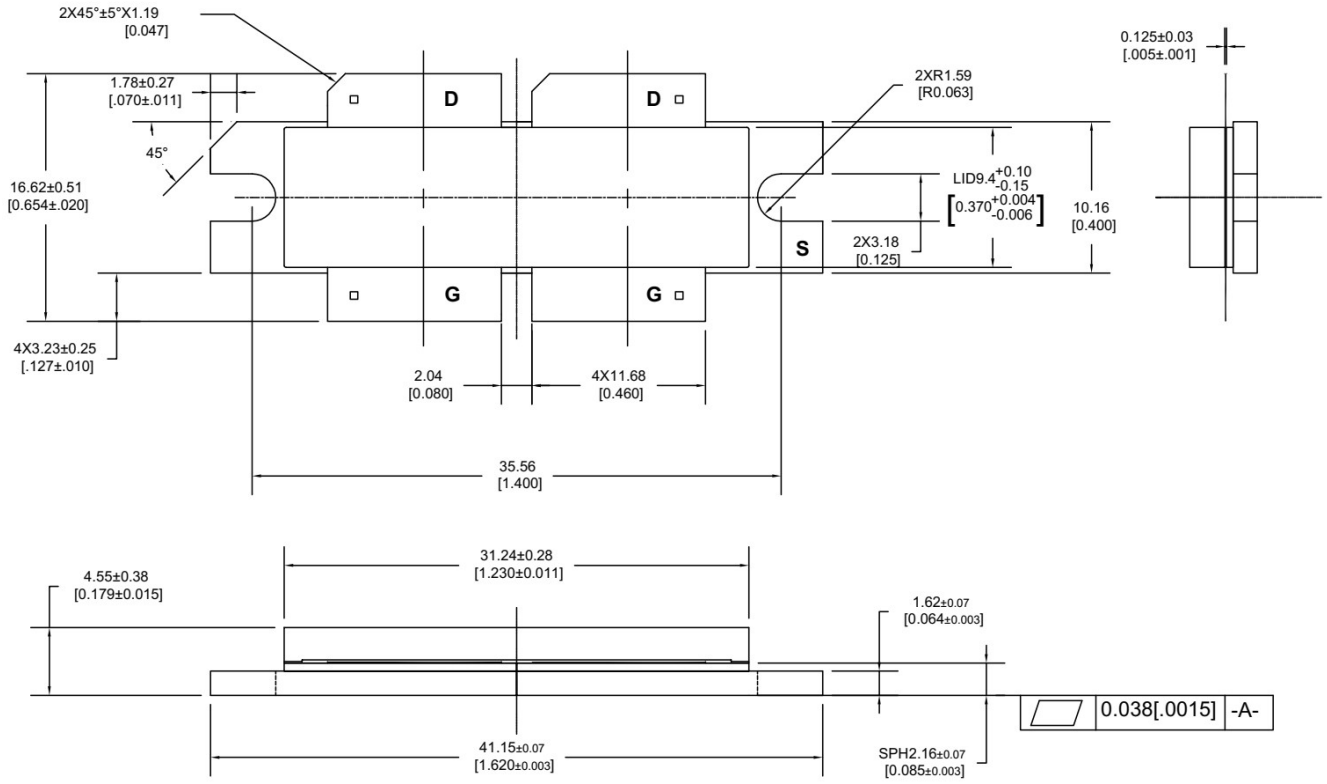
Figure 2: Power Efficiency as a Function of Pout

Vds = 50 V, Idq = 100 mA, TA = 25 °C, CW Frequency=100MHz

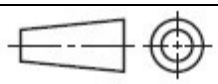


Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Unit: mm[Inches]
Unless otherwise specified tolerance: ±0.12mm

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					05/06/2020

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/10/15	Rev 1.0	Preliminary Datasheet
2023/11/28	Rev1.1	Add more application data

Application data based on TC-23-20,HL-23-11

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