



## 3400-3600MHz, 80W, 28V RF LDMOS FETs

### Description

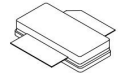
The ITCH36080B2 is a 80-watt, internally-matched LDMOS FETs, designed for cellular application with frequencies from 3400 to 3600MHz. It can biased at class AB or Class C for linear or pulse application as well

- Typical Performance of Demo (On Innogrations fixture with device soldered):

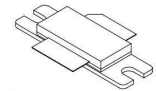
$V_{DD} = 28$  Volts,  $I_{DQ} = 450$  mA, Pulse Width=20 us, Duty cycle=10% .

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
3400	48.76	75.2	49.2	13.69	49.52	89.6	49.5
3500	49.47	88.5	49.2	13.72	50.21	104.9	50.2
3600	48.92	78.0	46.2	13.66	49.63	91.8	48.0

ITCH36080B2



ITCH36080B2E



- Typical Single-Carrier W-CDMA Performance (On Test Fixture with device soldered):

$V_{DD} = 28$ Volts,  $I_{DQ} = 800$  mA, WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz, PAR =10.5 dB at 0.01 % probability on CCDF.

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Eff (%)
3400	38	10.15	-42.3	15.3	14.8
3500	38	10.52	-40.5	15.1	13.8
3600	38	10.27	-42.6	15.0	13.4
3400	39	9.75	-41.7	15.3	17.0
3500	39	10.23	-40.0	15.1	15.8
3600	39	9.70	-41.6	15.0	15.3

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCl drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+32	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C



**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC test	$R_{\theta JC}$	0.35	$^\circ\text{C/W}$

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**DC Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$			100	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$			1	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 10\text{V}$ , $V_{DS} = 0\text{V}$ )	$I_{GSS}$			1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 28\text{V}$ , $I_D = 300\mu\text{A}$ )	$V_{GS(th)}$		2.2		V
Gate Quiescent Voltage ( $V_{DD} = 28\text{V}$ , $I_D = 450\text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$		2.6	3.5	V

**Functional Tests** (In Innogrations Test Fixture, 50 ohm system)  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 450\text{mA}$ ,  $f = 3500\text{MHz}$ , Pulsed CW Signal Measurements.

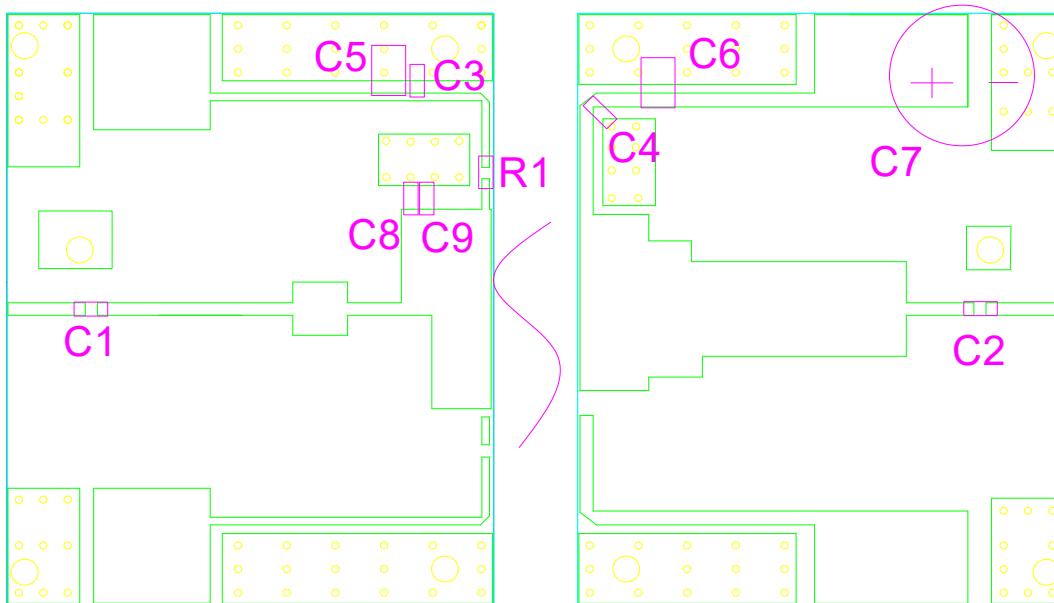
Pulse width: 20uS, duty cycle: 10%

Power Gain	$G_p$		13.5		dB
3 dB Compression Point	$P_{3dB}$		80		W
Drain Efficiency@P3dB	$\eta_D$		50		%
Input Return Loss	IRL		-10		dB

**Load Mismatch (In Innogrations Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 450\text{mA}$ ,  $f = 3500\text{MHz}$

VSWR 10:1 at 10W WCDMA Output Power	No Device Degradation
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**Reference Circuit of Test Fixture Assembly Diagram**



**Figure 1. Test Circuit Component Layout (PCB RO4350B 20mils)**

**Table 5. Test Circuit Component Designations and Values**

Designator	Footprint	Comment	Quantity
C1, C2, C3, C4	0603	8.2pF	4
C5, C6	1210	10uF/100V	2
C7		220uF/63V	1
C8	0603	2.7 pF	1
C9	0603	1.5 pF	1
R1	0603	10R	1

### TYPICAL CHARACTERISTICS

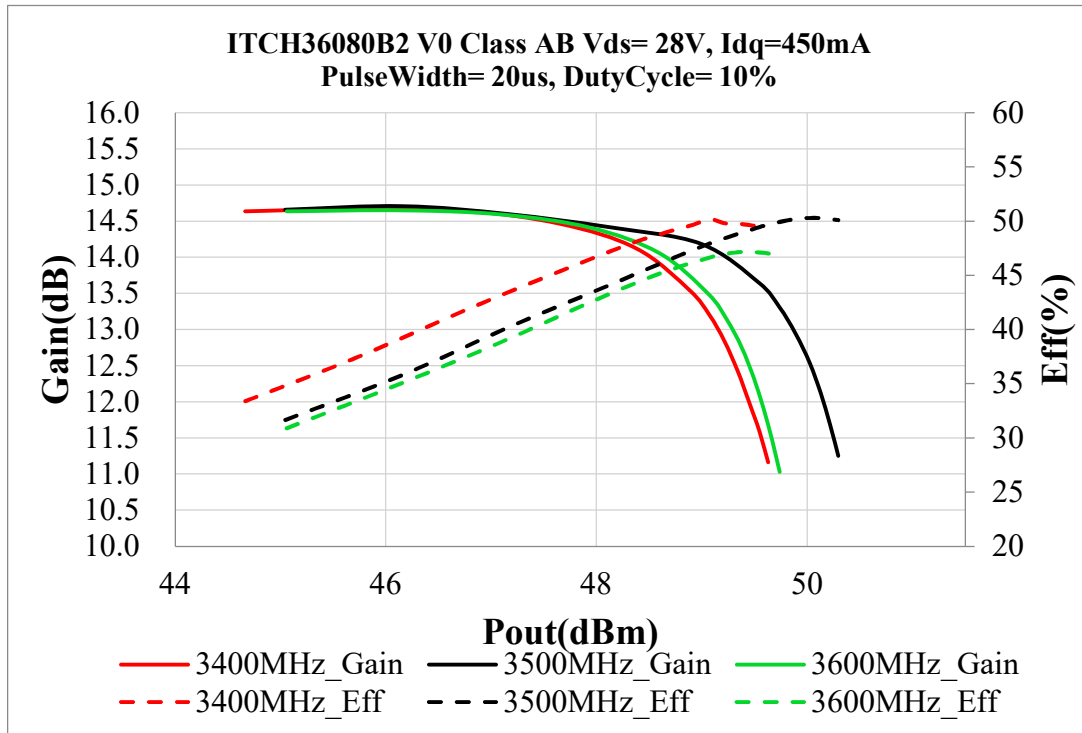


Figure 2. Power gain and drain efficiency as function of pulsed CW Pout

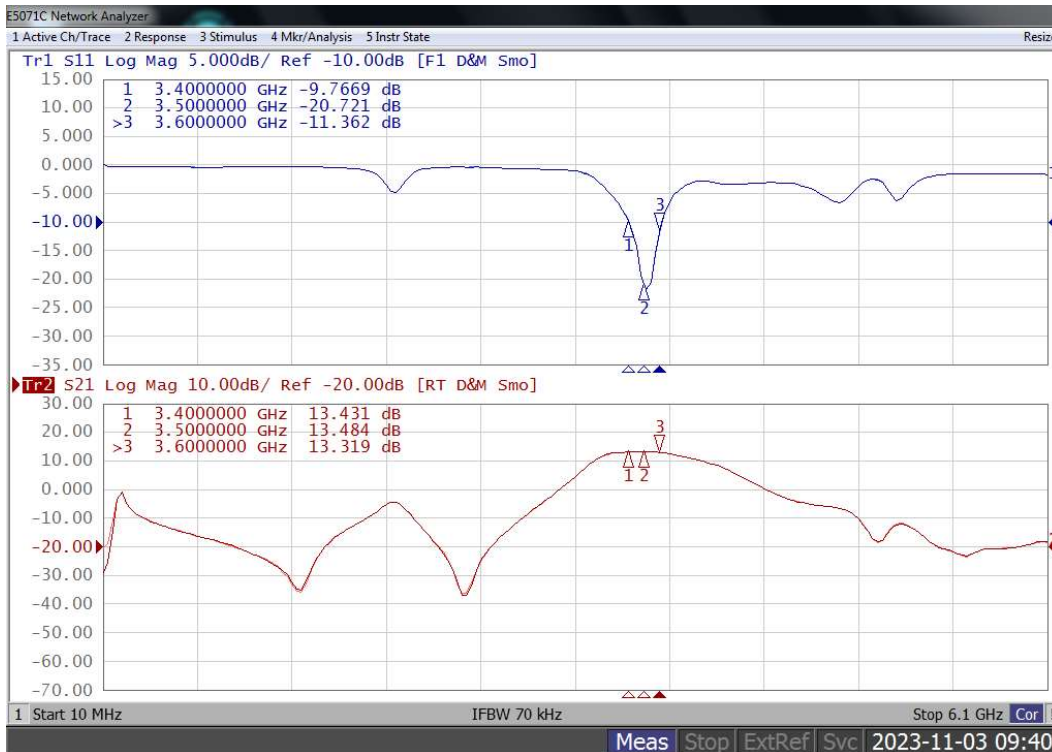
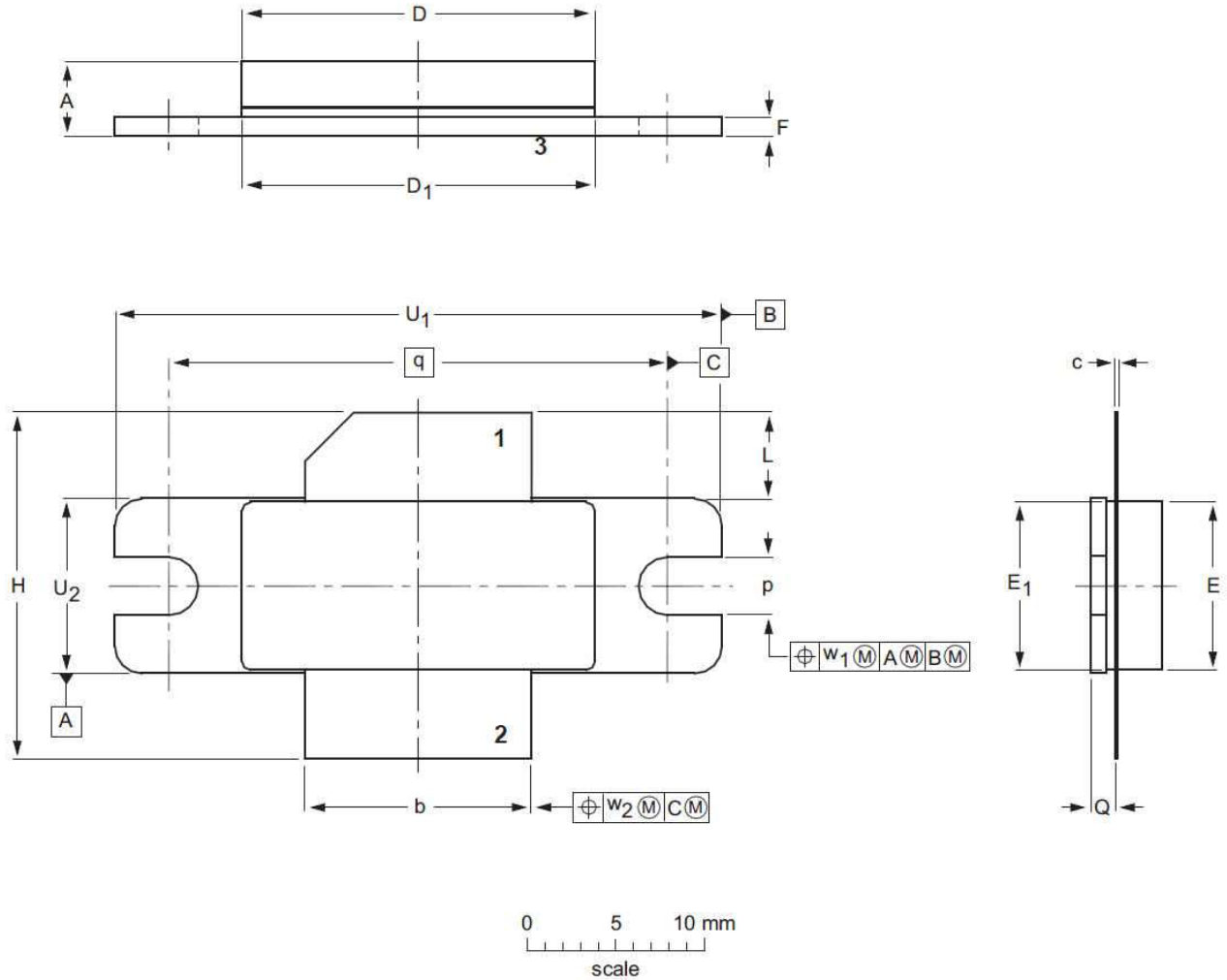


Figure 3. Broadband Frequency Response



## Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)

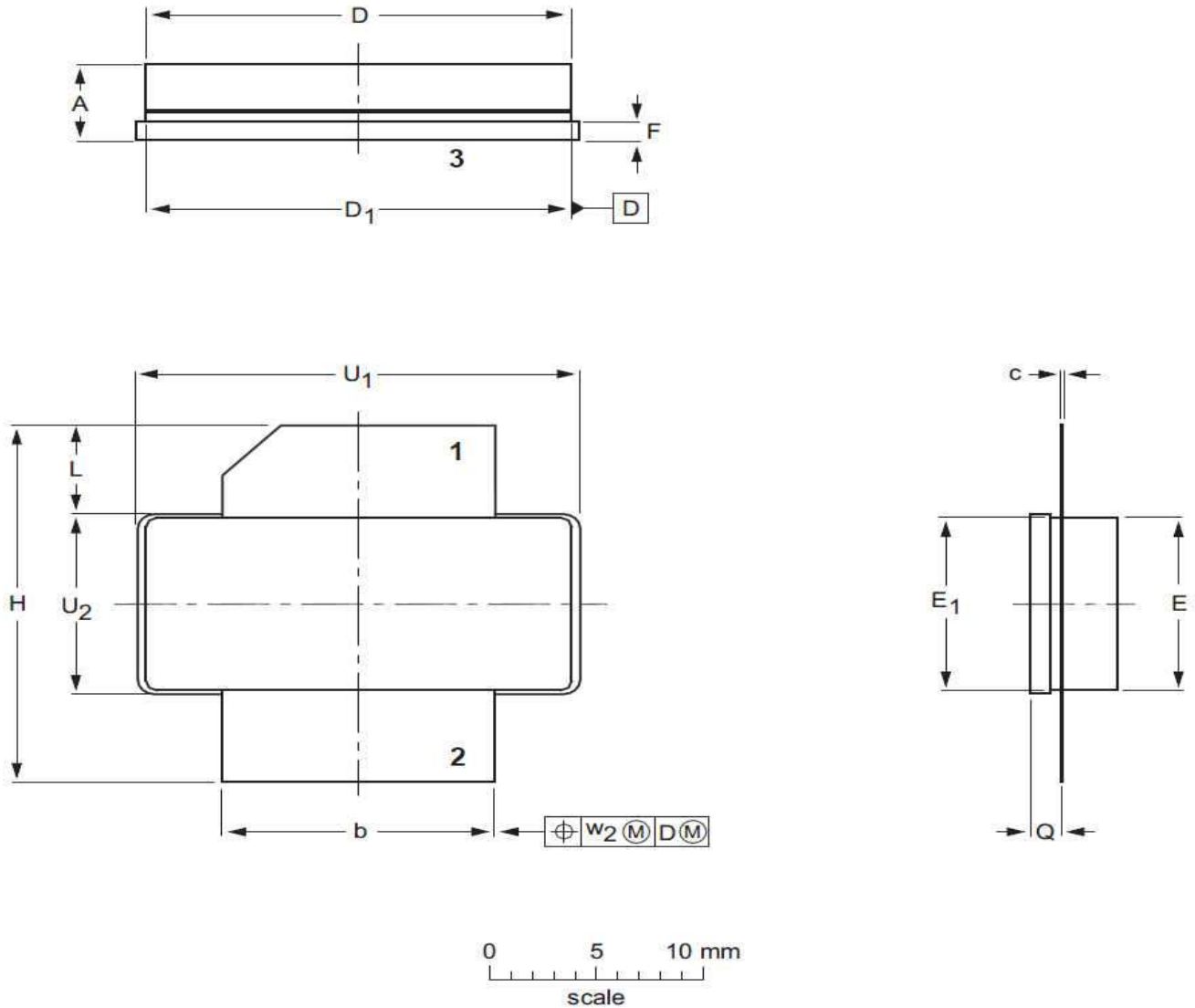


UNIT	A	b	c	D	$D_1$	E	$E_1$	F	H	L	p	Q	q	$U_1$	$U_2$	$W_1$	$W_2$
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013



Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
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PKG-B2					03/12/2013



## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/11/3	Rev 1.0	Preliminary Datasheet Creation

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