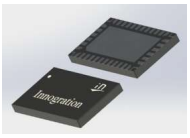
40W,28V Plastic RF LDMOS Transistor

ITEH27041C6



Description

The ITEH27041C6 is a dual path 40-watt, highly rugged, LDMOS transistor, designed for driver applications at frequencies from 2.3 to 2.7GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as highly compact Doherty ,ideal for high efficiency and low cost, DPD friendly driver for 4G/5G application within 2.3-2.7GHz.

- Typical 2.6GHz Doherty RF Performance (On Innogration fixture with device soldered).

Vds=28V Idq_main=150mA, Vgs_peak=1.8V

Freq (MHz)	Pulse CW Signal			P_{avg}=35dBm WCDMA Signal		
	P1dB Gain (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	$ACPR_{5M}$ (dBc)
2500	13.39	51.60	58.39	15.0	26.22	-39.37
2600	14.37	50.35	59.55	16.0	26.39	-36.80
2700	14.04	43.13	57.65	16.0	26.03	-39.88

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- L, S band power ampliifer
- All 4G/5G cellular application within 2.3-2.7GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

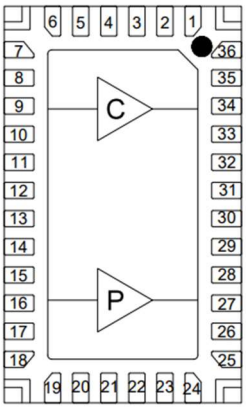
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	V_{GS}(th)	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 180mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.7	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 150 mA, f = 2700 MHz

VSWR 10:1 at 40W pulse CW Output Power	No Device Degradation

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for main path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for Main path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

2500-2700MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

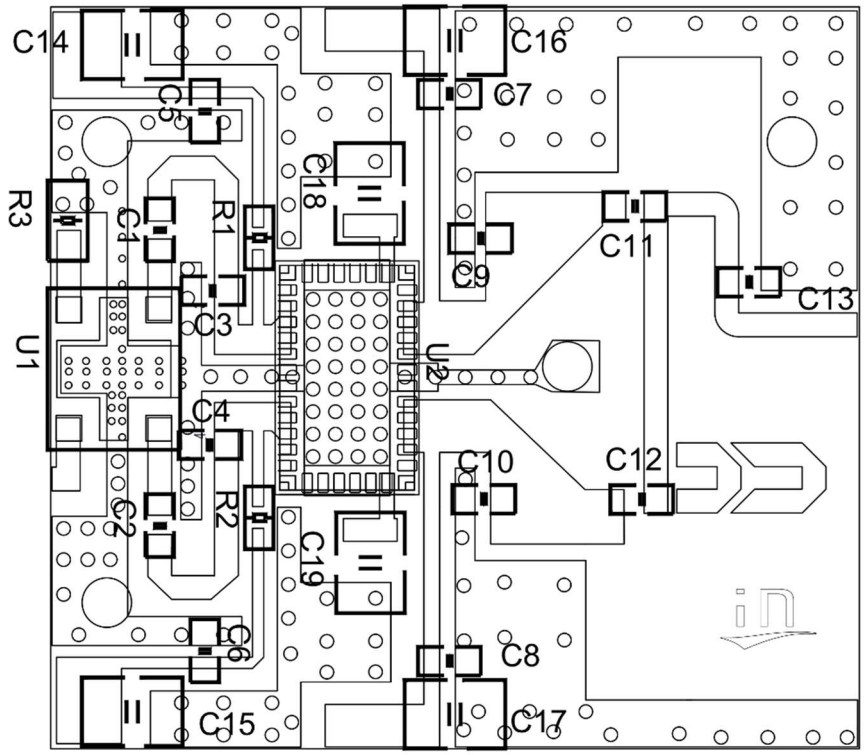


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C5, C6, C7, C8, C12	0603	8.2pF/250V	7
C3	0603	2.2pF/250V	1
C4	0603	2.4pF/250V	1
C9	0603	0.8pF/250V	1
C10	0603	0.6pF/250V	1
C11	0603	6.8pF/250V	1
C13	0603	0.3pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	0805	51R	1
U1	6.35*5.08mm	HC2500P03	1
U2	C6	ITEH27041C6	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output at Idq=150mA

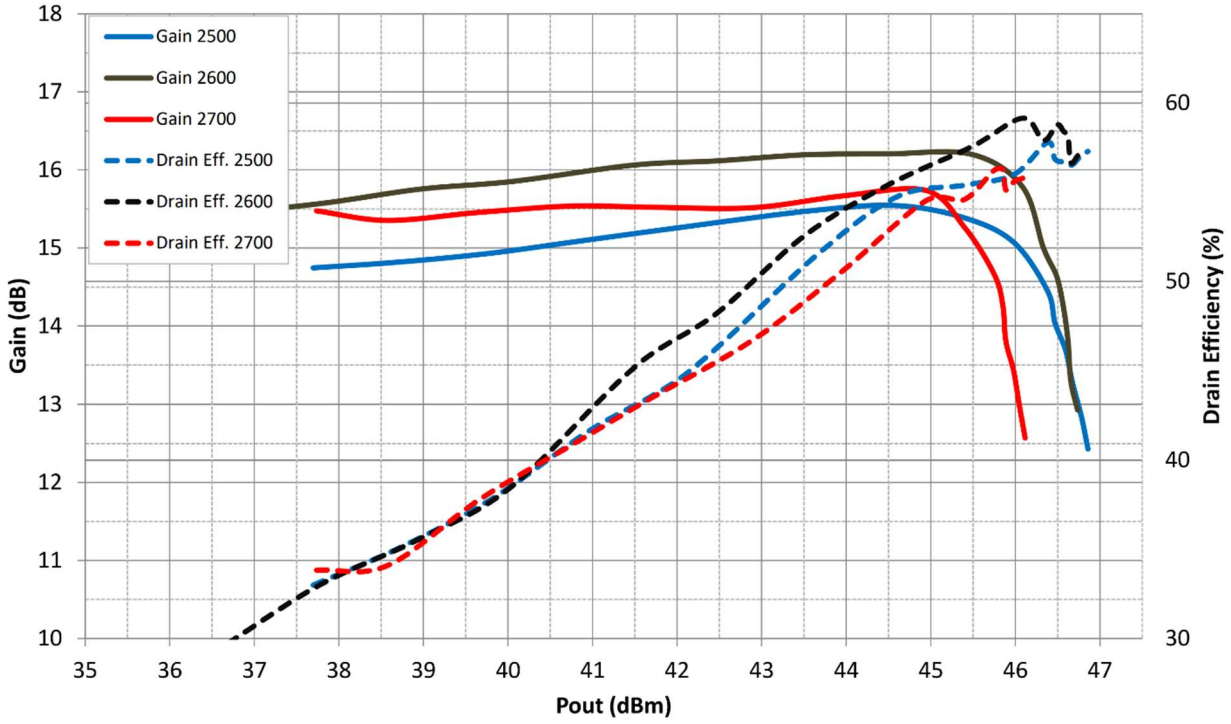
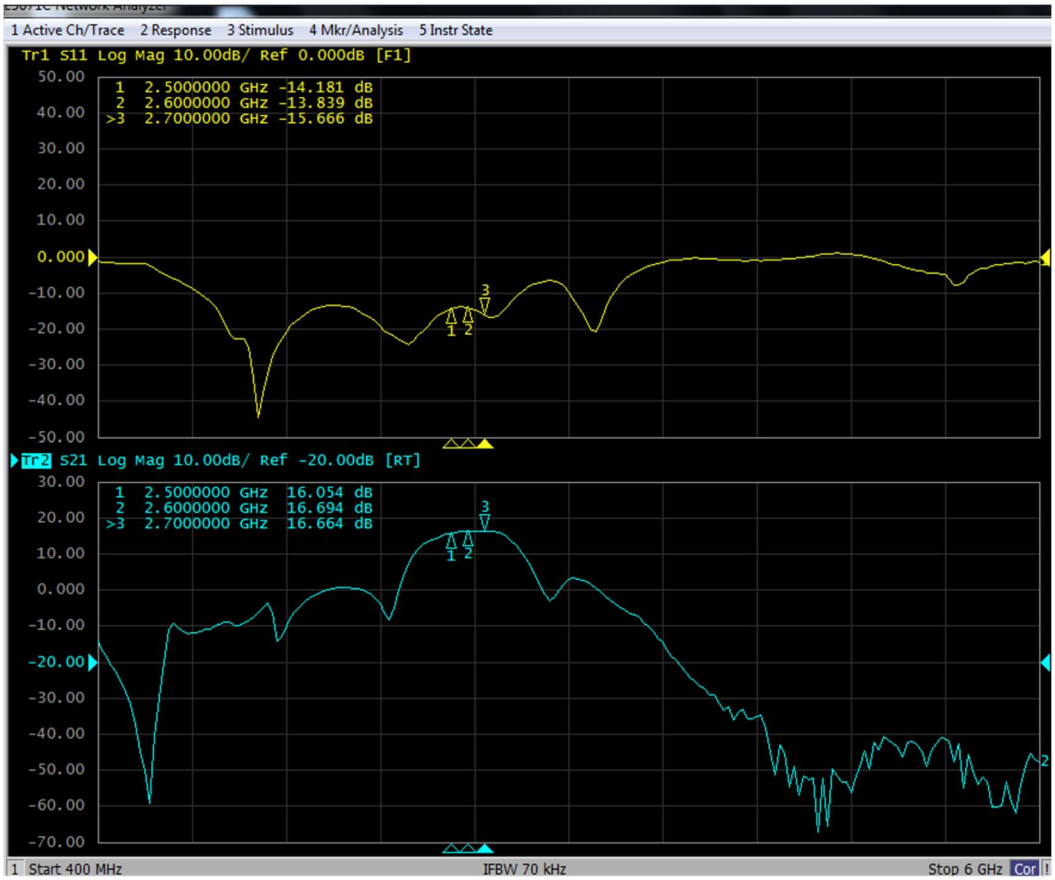
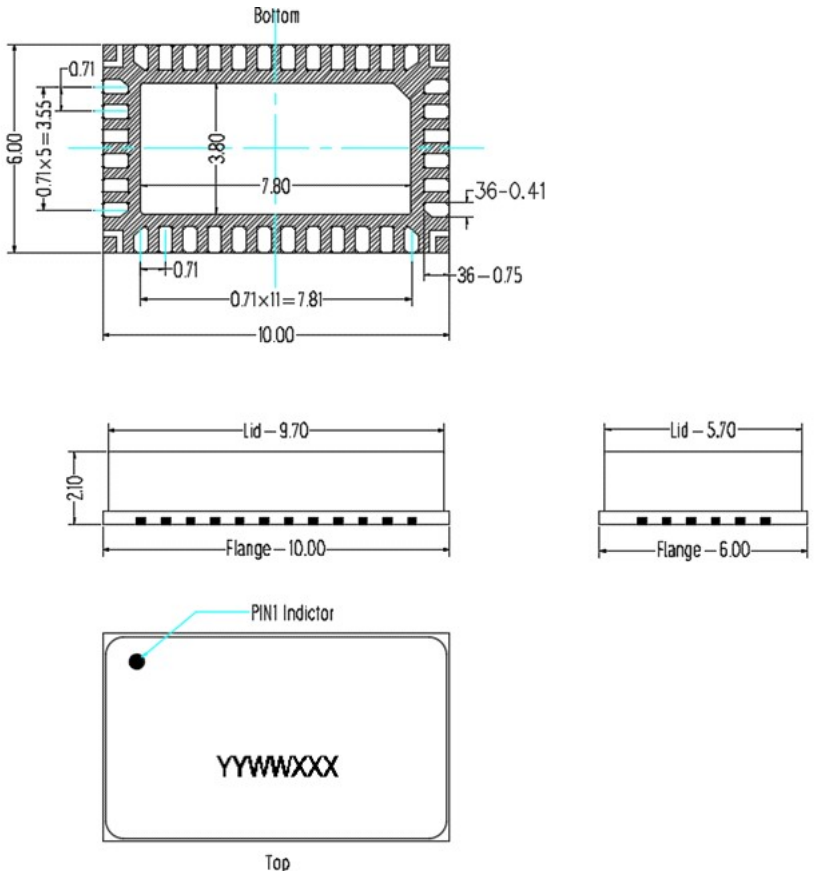


Figure 4.Network analyzer output S11/S21



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/11/2	**Rev 1.0**	**Preliminary Datasheet**

Application data based on ZBB-23-32

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