

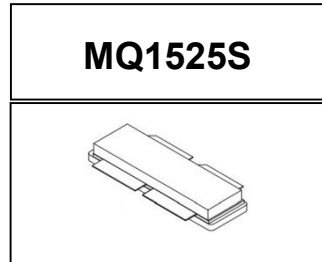
# MQ1525S LDMOS TRANSISTOR

Document Number: MQ1525S  
Preliminary Datasheet V1.0

## 200W, 28V , 0.8-1.4GHz Full Band RF LDMOS FETs

### Description

The MQ1525S is a 200-watt capable, high performance, input matched push pull LDMOS FET, for wide-band commercial and industrial applications with frequencies 800 to 1400MHz. It can be used for both CW and pulse application or any other modulation signal. When operated at higher voltage 32V, it can deliver typically 250W within the band



- Typical CW Performance at 28V (On Innogration 0.8-1.4GHz wideband fixture with device soldered):

MQ1525S Vds=28V Idq=200mA Vgs=2.5V CW							Harmonics (Pout=Pout)	
F(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	I(A)	Gain(dB)	Eff(%)	2th(dBc)	3th(dBc)
800	44.6	54.4	277	20.30	9.8	48.8	-26.2	-19.8
900	45.2	53.5	224	17.60	8.3	45.4	-30.6	-24.3
1000	45	53.4	219	18.50	8.4	42.2	-20.7	-60
1100	44.7	53.1	204	18.50	8.3	40.2	-43.4	-32.3
1200	44.6	53.8	244	20.60	9.2	42.3	-21.3	-35
1300	44.5	54.0	251	21.20	9.5	42.3	-18	-56
1400	44.4	53.1	204	18.20	8.7	40.1	-41	-37

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCl dri
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- P band CW amplifier
- L band CW amplifier
- Jammer
- Data link

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+65	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+32	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>j</sub>	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T <sub>c</sub> = 85°C, T <sub>j</sub> =200°C, DC test	R <sub>θJC</sub>	0.2	°C/W

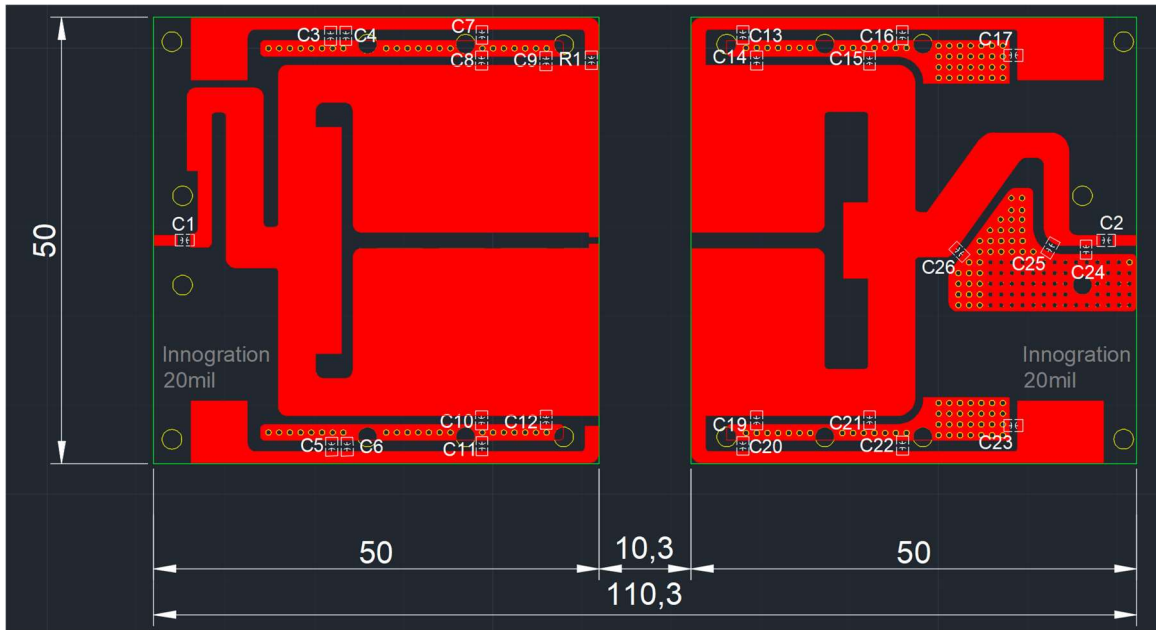
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**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Reference Circuit of Test Fixture Assembly Diagram  
(Layout file upon request, 20mil RO4350)**

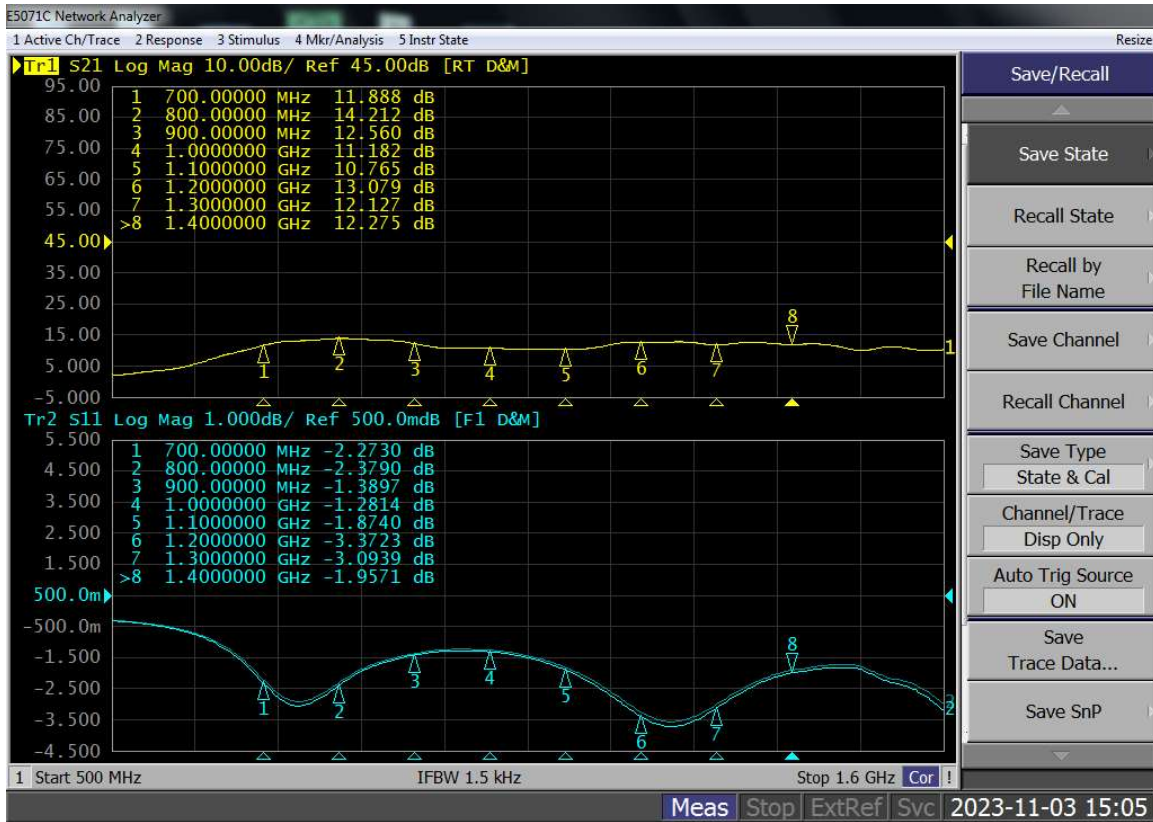


**Table 5. Test Circuit Component Designations and Values**

Part	description	Model
C1,C2	56PF MQ101111	
C3,C5	22uF 0805	Chip Resistor
C17,C23	10uF/1210	Ceramic multilayer capacitor
R1	10Ω 0805	Chip Resistor
C4,C6	1000PF MQ300805	
C7,C11,C16,C22	75PF MQ301111	
C8,C10,C13,C20	2.7PF MQ301111	
C9,C12,C14,C19	2.2PF MQ301111	
C15,C21	3.6PF MQ301111	
C24,C25	0.5PF MQ301111	
C26	1.2PF MQ301111	
PCB	Rogers 4350 20mil	

## TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 ( $V_{ds}=28V$   $I_{dq}=1.5A$ )

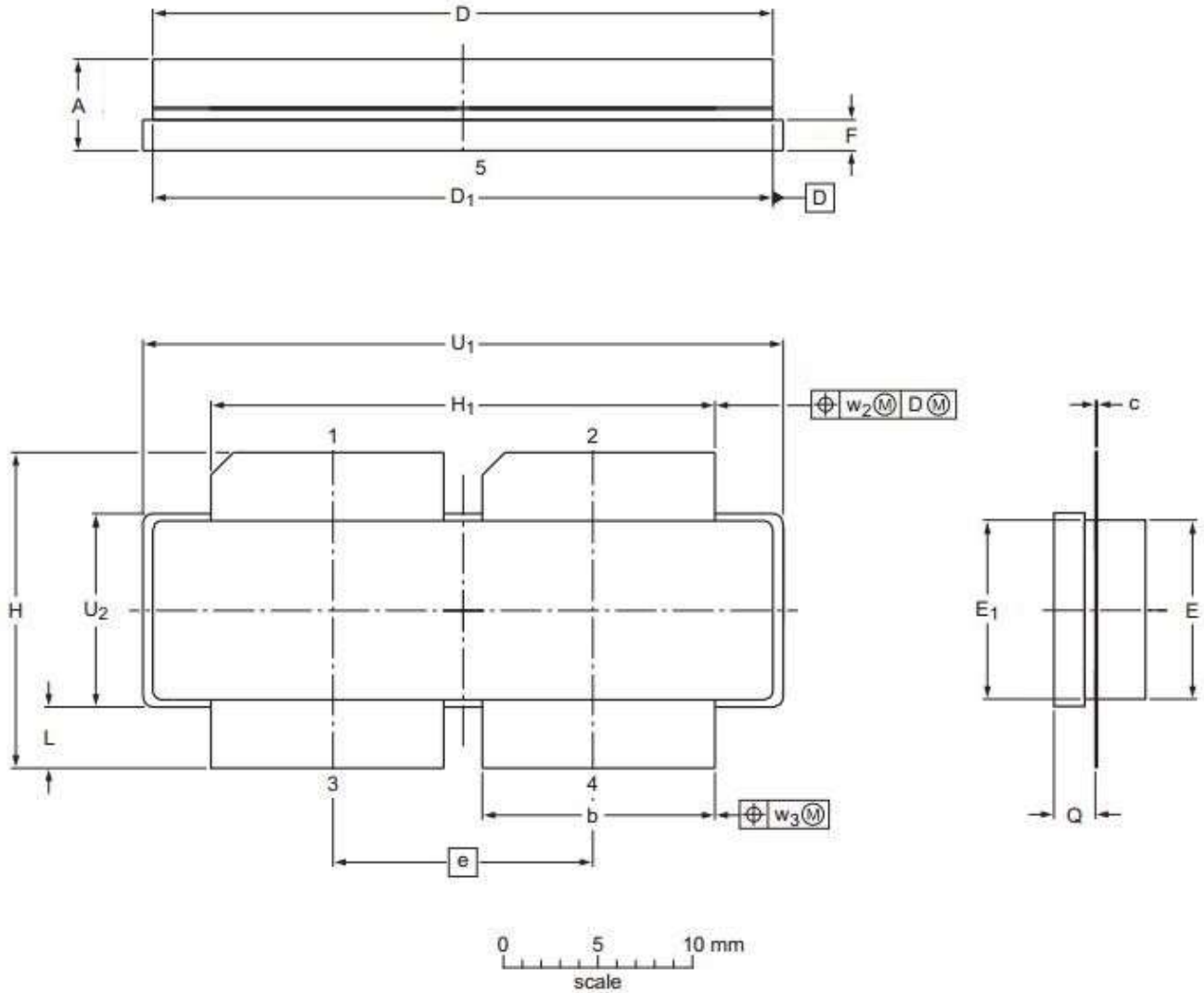


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## Package Outline

Earless flanged ceramic package; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

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## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/7/14	Rev 1.0	Preliminary Datasheet

Application data based on SYX-23-56

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