



30W,13.6V High Power RF LDMOS FETs

ITEH09100C6

Description

The ITEH09100C6 is a 30-watt, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications at frequencies up to 1GHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format. It is also featured by its lower cost of plastic open cavity for surface mount on PCB through vias



- Typical LMR UHF CW Performance (On Innegration fixture with device soldered).

ITEH09100C6 VGS=2.47V VDS=13.6V IDQ=100mA CW						
Freq(MHz)	Pout(dBm)	Pout(W)	IDS(A)	Pin(dBm)	Gain(dB)	Eff(%)
400	45.16	32.8	4.1	33.79	11.37	58.84
420	45.9	38.9	4.54	32.36	13.54	63.01
440	45.02	31.8	4.24	32.36	12.66	55.09
460	45.28	33.7	4.5	32.59	12.69	55.11
470	45.68	37.0	4.82	31.34	14.34	56.42
480	45.21	33.2	4.82	31.8	13.41	50.63

Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Pb-free, RoHS-compliant

Suitable Applications

- VHF/UHF Land mobile radio (LMR)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^\circ\text{C}$, $T_j=200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2



Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		70		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 13.6V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 9 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 13.6V, I _D = 600 μA)	V _{GS(th)}	—	2	—	V
Gate Quiescent Voltage (V _{DD} = 13.6V, I _D = 100mA, Measured in Functional Test)	V _{GS(Q)}	—	2.86	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): V_{DD} = 13.6Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 10:1 at 30W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Definition(Top View)



Pin No.	Symbol	Description
1-7,12,13,18-25,30,31,36	GND	DC/RF Ground
8,9,10,11,14,15,16,17	Vgs/RF In	Vgs and RF input
26,27,28,29,32,33,34,35	Vds/RF out	Vds and RF output
Package Base	GND	DC/RF Ground.

**Reference Circuit of Test Fixture Assembly Diagram
400-470MHz RO4350B 30mils**

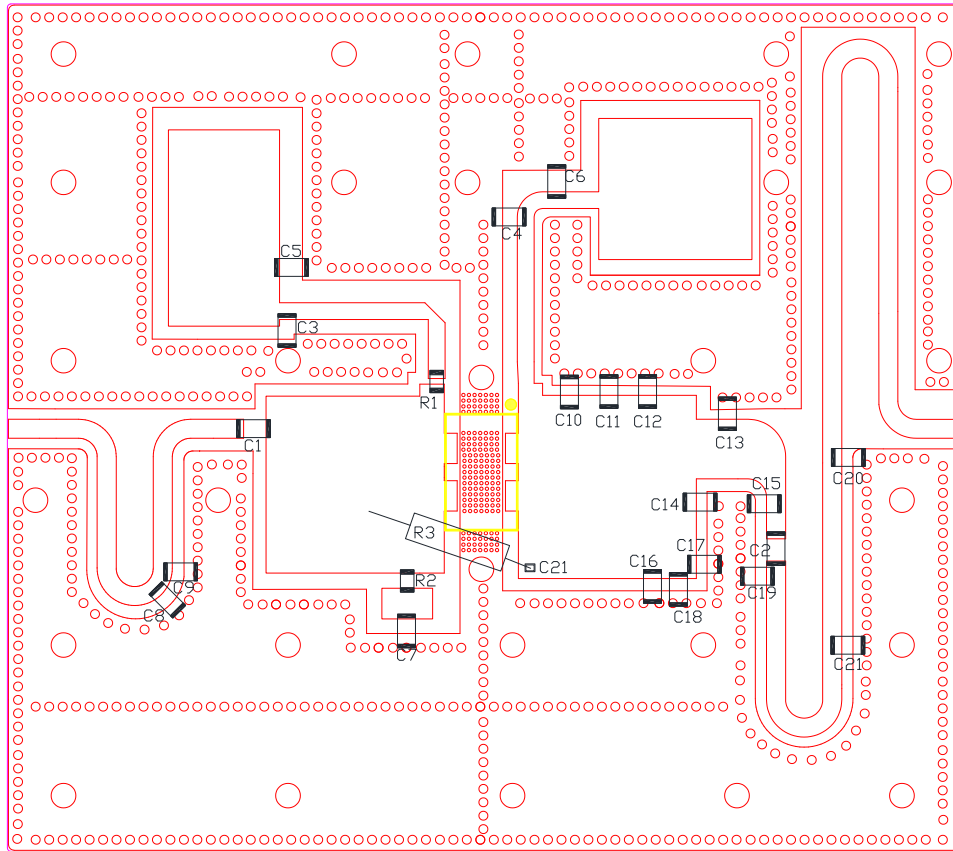


Figure 5. Test Circuit Component Layout

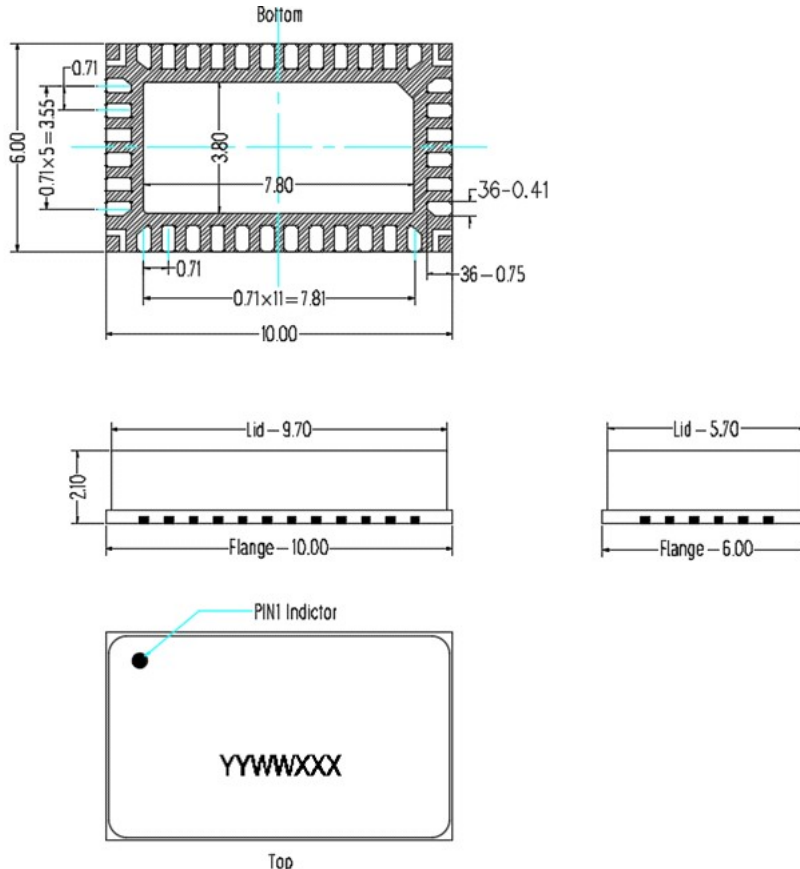
Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1,C2,C3,C4	200pF	DLC70B
C5,C6,C7,C21	10uF/50V	10uF/50V
C8,C9,C17,C18,C15	10pF	DLC70B
C10,C11,C12,C13,C14,C16,C19,C20,C21	5.6pF	DLC70B
R1,R2	Chip Resistor,9.1ohm	1206
R3	330 Ω	



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/1/17	Rev 1.0	Preliminary Datasheet

Application data based on HL-23-02

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