



40W,28V Plastic RF LDMOS Transistor

ITEH09041C6

Description

The ITEH09041C6 is a dual path 40-watt, highly rugged, LDMOS transistor, designed for driver applications at frequencies from 0.7 to 1.0GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as highly compact Doherty ,ideal for high efficiency and low cost, DPD friendly driver for 4G/5G application within 0.7-1.0GHz.



- Typical 700MHz Doherty RF Performance (On Innegration fixture with device soldered).

V_{ds}=28V I_{dq_main}=30mA, V_{gs_peak}=1.6V

Freq (MHz)	Pulse CW Signal			P _{avg} =36dBm WCDMA Signal		
	P1dB Gain (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
758	13.8	45.0	65.2	14.3	43.5	-29.6
780	14.43	46.0	67.4	15.0	43.4	-29.6
803	14.56	42.8	66.7	15.1	41.4	-29.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.7 to 1.0GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.45	°C/W

Table 3. ESD Protection Characteristics

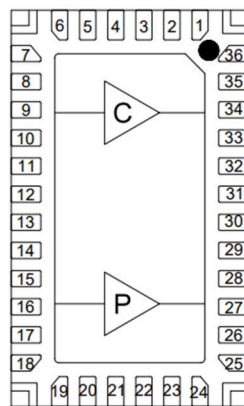
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2



Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=100\mu A$	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11V, V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28V, I_D = 600\mu A$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 28V, I_D = 180mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.7	—	V
Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 28Vdc, I_{DQ} = 180mA, f = 2200MHz$					
VSWR 10:1 at 40W pulse CW Output Power	No Device Degradation				

Figure 1: Pin Connection definition
Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for main path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for Main path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

758-803MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

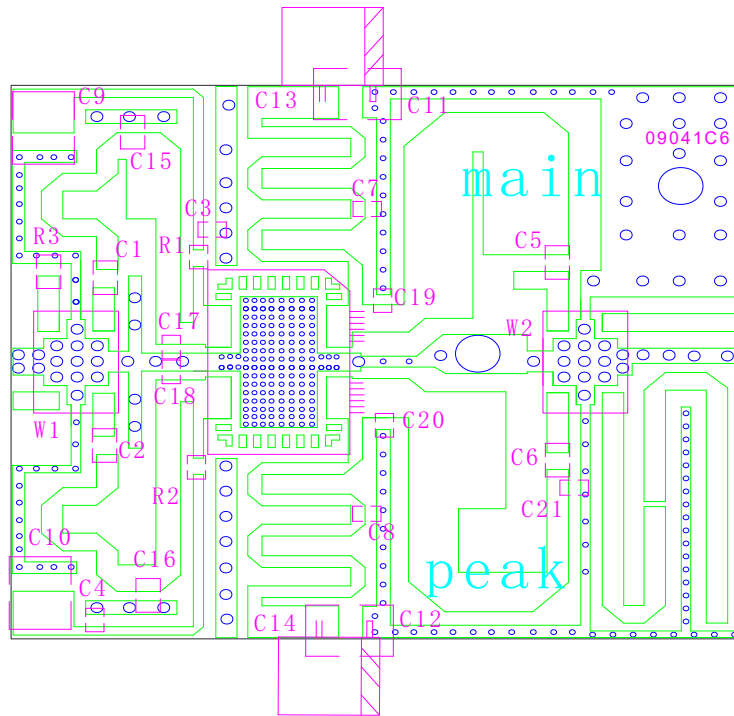


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1, C2,	10pF	0402/0603	2
C3, C4, C5, C6, C7, C8	68pF	0402/0603	6
C9, C10, C11, C12	10uF/100V	1210	4
C13, C14	100uF/63V		2
C15	8.2pF	0402/0603	1
C16	6.8pF	0402/0603	1
C17, C18	18 pF	0402/0603	2
C19	1.0pF	0402/0603	1
C20	4.7pF	0402/0603	1
C21	2.0pF	0402/0603	1
R1, R2	10 Ω	0402/0603	2
R3	51 Ω	0805	1
W1, W2	HC07F03		2

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=180mA

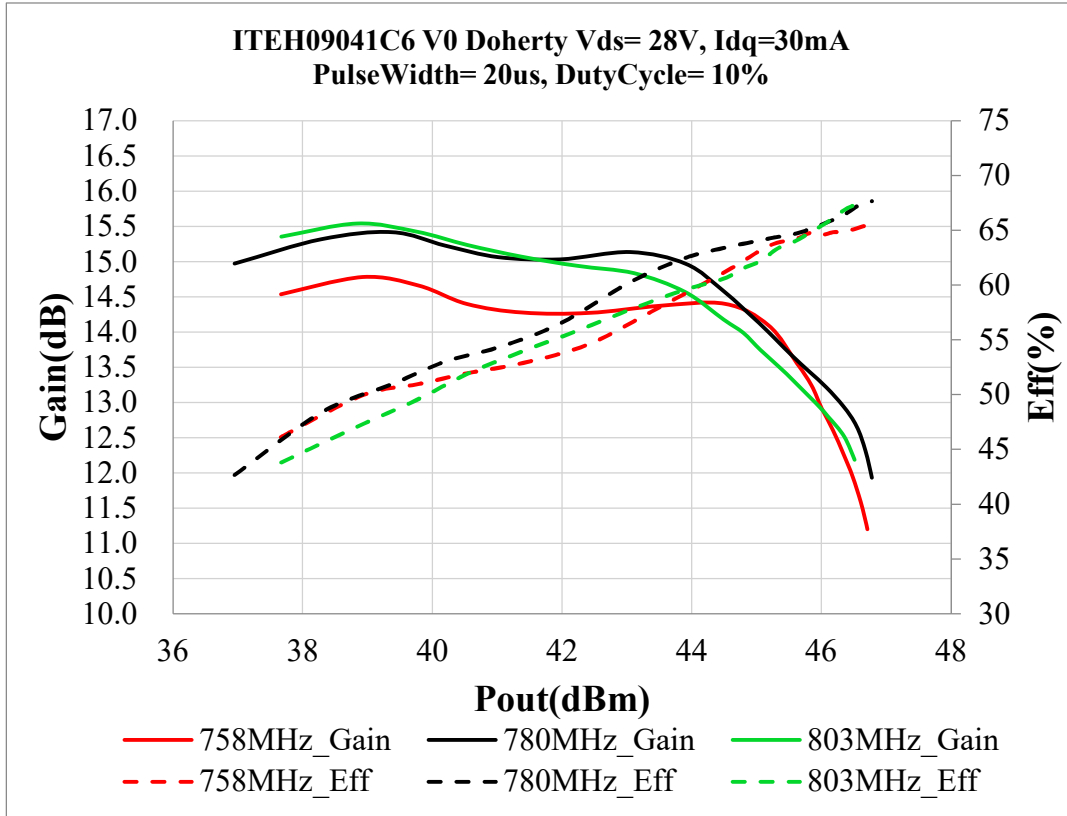
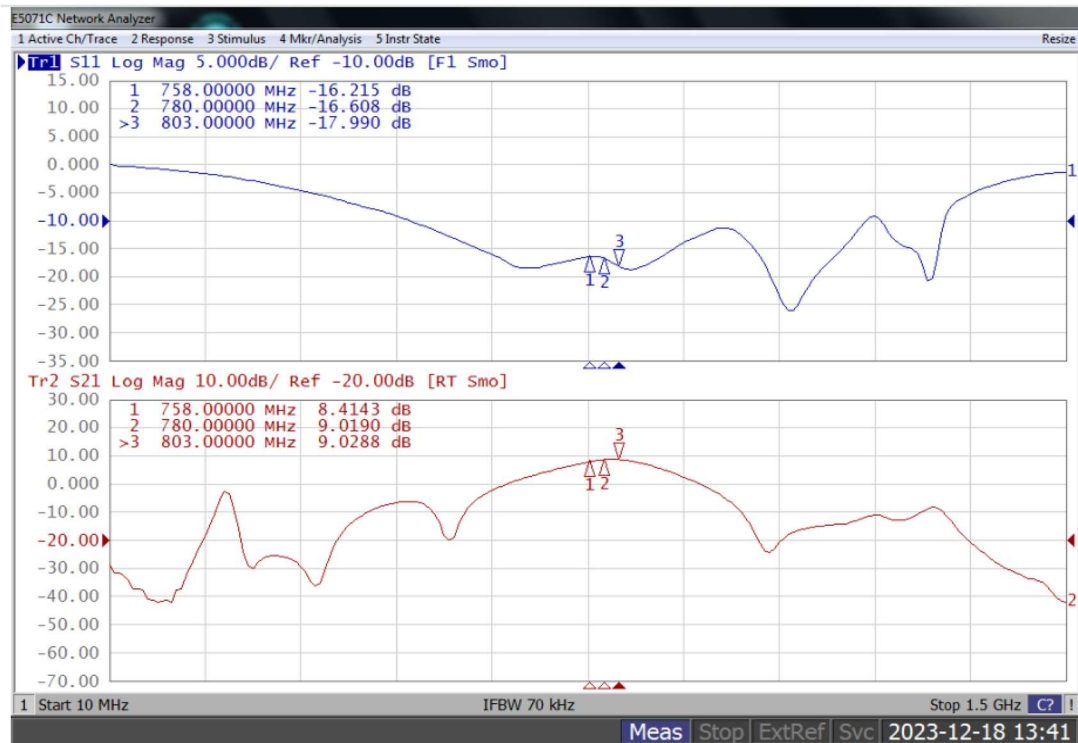


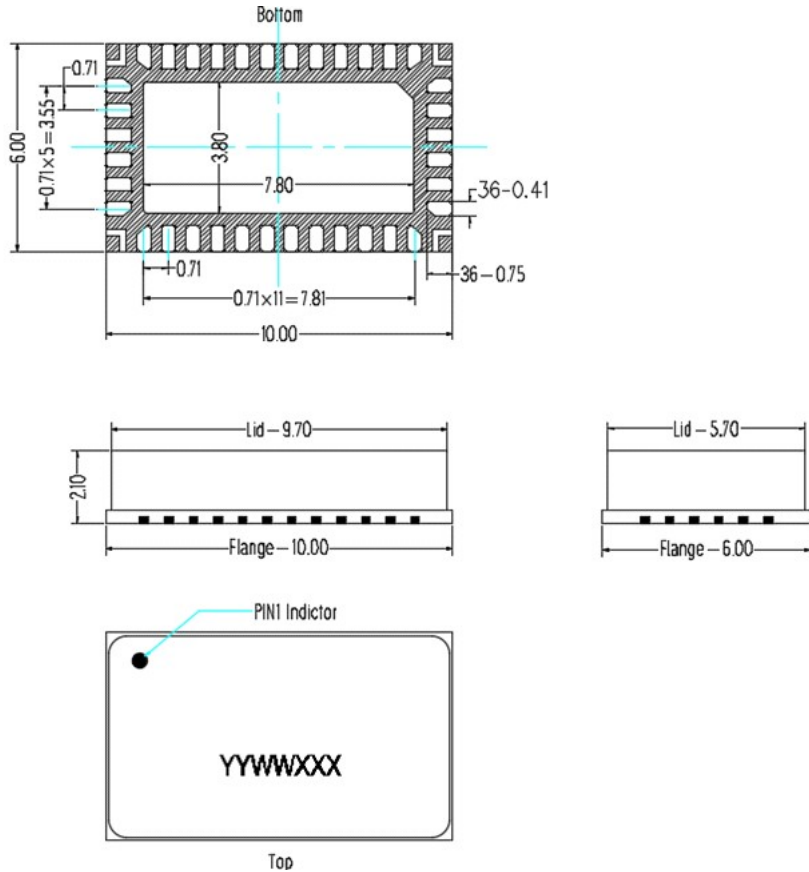
Figure 5. Network analyzer output S11/S21





Package Dimensions

10*6 Plastic Package



Notes:

- 1. All dimensions are in mm;
- 2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/12/18	Rev 1.0	Preliminary Datasheet

Application data based on LSM-23-38

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