

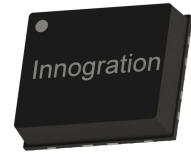
ITEV10250C9 LDMOS TRANSISTOR

Document Number: ITEV10250C9
Preliminary Datasheet V1.0

120W, 28V High Power RF LDMOS FETs

ITEV10250C9

Description



The ITEV10250C9 is a 120-watt capable, high performance, internally matched LDMOS FET, designed for applications with frequencies 0.7 to 1GHz, in 12*10mm QFN plastic package,

It can be soldered on PCB through high density grounding vias for pulse or back off linear application or soldered directly on heatsink. for CW application

- Typical performance(on Innogrations test board with device soldered on PCB through high density vias)
Vds=28V, Idq=720mA, 10% 100us

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
758	50.27	106.5	49.2	17.07	51.95	156.6	57.5
780	49.7	93.4	52.3	17.09	51.37	137.2	59.6
803	48.8	75.8	53.0	16.28	50.42	110.1	57.9

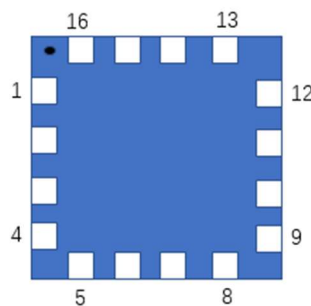
Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application up to 1Hz

Pin Configuration and Description (Top view)



Pin No.	Symbol	Description
5-8	RF IN/Vgs	RF Input/Gate bias
13-16	RF OUT/Vds	RF Output/Drain bias
Others	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.75	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{mA}$	$V_{(BR)DS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_D = 720\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.5	—	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 720\text{mA}$, $f = 700\text{MHz}$, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 120W Pulsed CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout

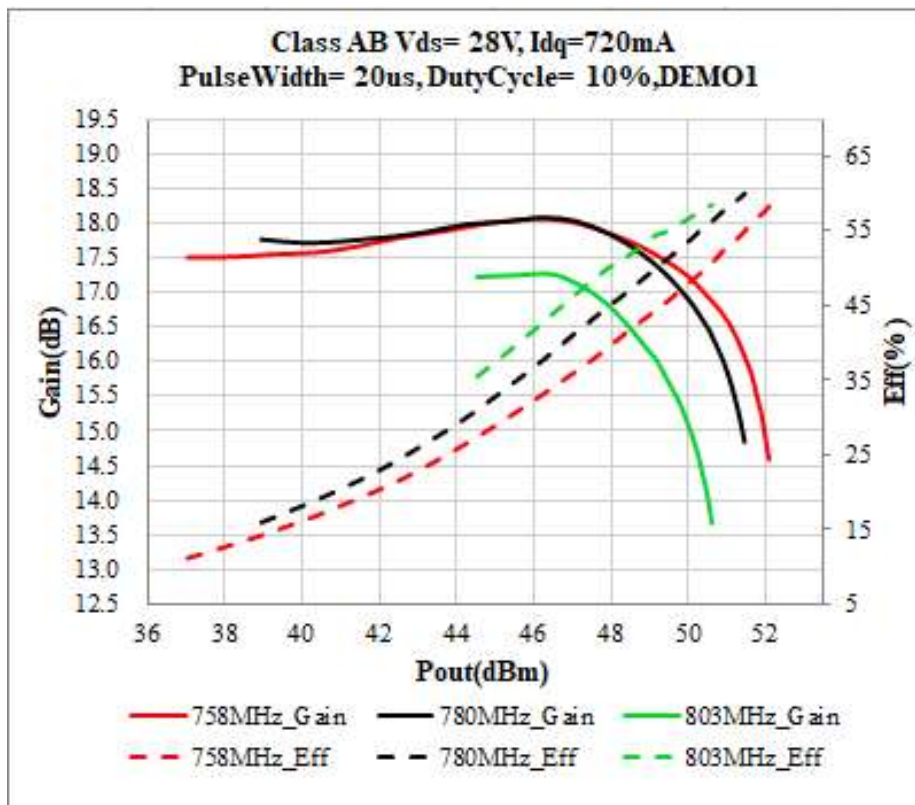
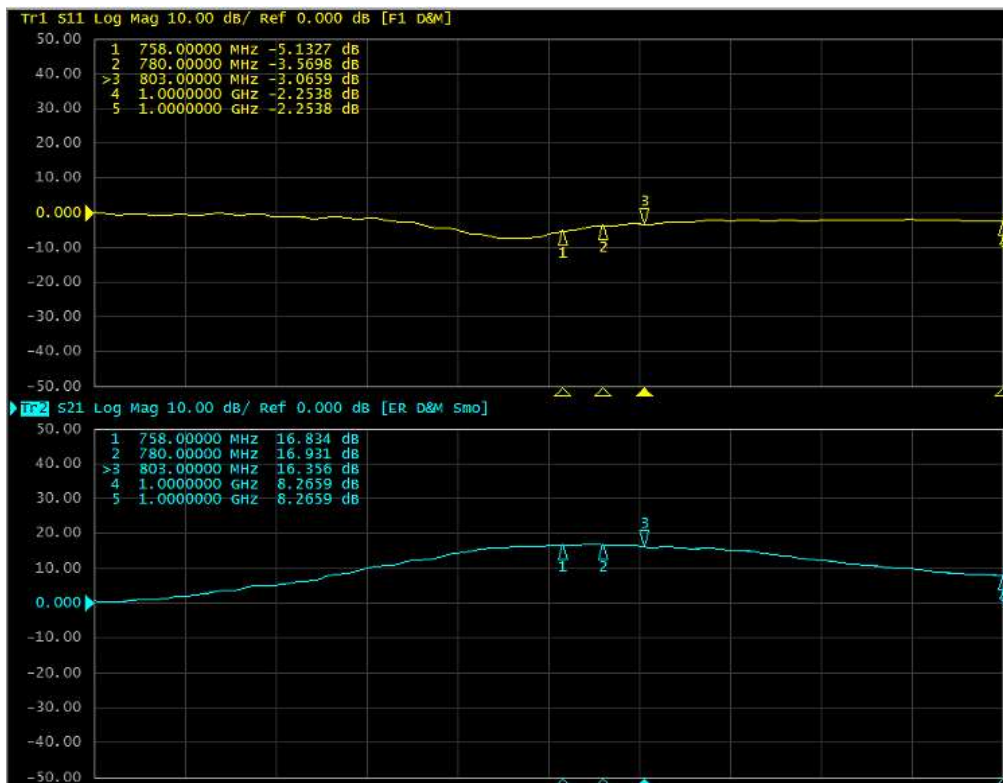


Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

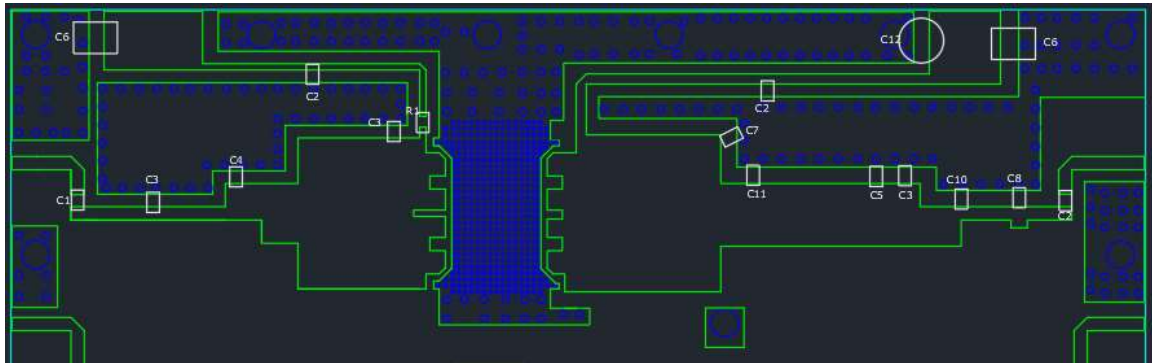
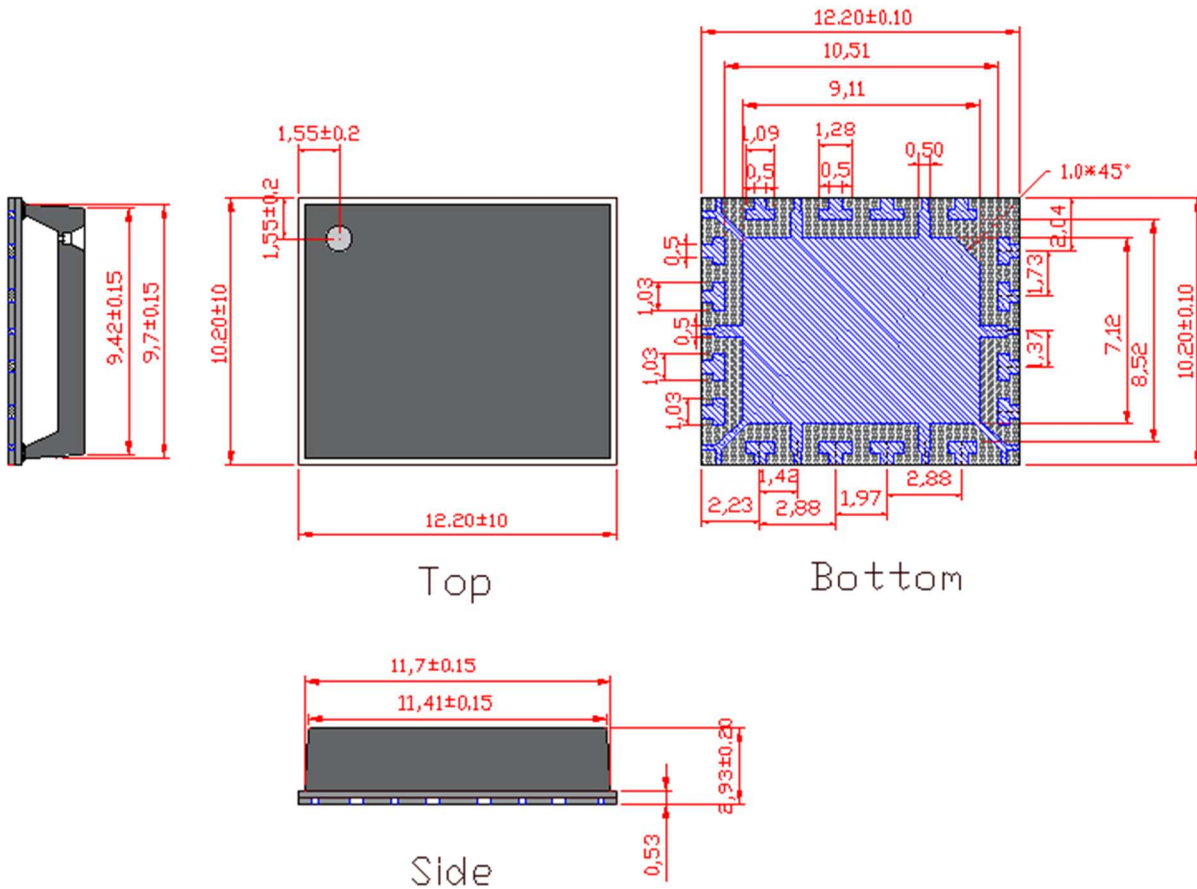


Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITEV10250C9	1
C1	3.9pF	1
C6	10uF/63V	2
R1	10 Ω	1
C12	470uF/63V	1
C2	100pF	3
C3	6.8pF	3
C4	3pF	1
C7	5.6pF	1
C10	4.7pF	1
C11	3.3pF	1
C8	0.3pF	1
C5	0.4pF	1
PCB	20mils RO4350B	

Package Dimensions (Unit:mm)



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/12/20	Rev 1.0	Preliminary Datasheet Creation

Application data based on ZYX-23-06

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