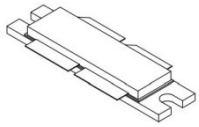
MQ161K0VP LDMOS TRANSISTOR

Document Number: MQ161K0VP
Preliminary Datasheet V1.0

1000W, 50V L band pulsed RF LDMOS FETs

MQ161K0VP



Description

The MQ161K0VP is a 1000W, high performance, internally matched LDMOS FET, designed for any applications with frequencies 1.3 to 1.6GHz.

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):
  Vds = 50 V, Idq = 100 mA, TA = 25 °C, 1.3GHz

Pulsed CW conditions	Pin(dBm)	Pout(dBm)	Pout(W)	Ids(A)	Gain(dB)	Eff(%)
8us,5%	49.54	61.32	1355	2.6	11.8	52
20us,20%	48.61	60.38	1100	8.6	11.8	51

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 1000W Pout, Pulse width: 8us, duty cycle: 5%, Vds=50 V, I_{DQ} = 100 mA	$R_{\theta JC}$	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage	V_{DSS}	115			V

(V_{GS}=0V; I_D=100uA)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Reference Circuit of Test Fixture

(Layout file upon request) PCB: Roger 4350B, 20mils

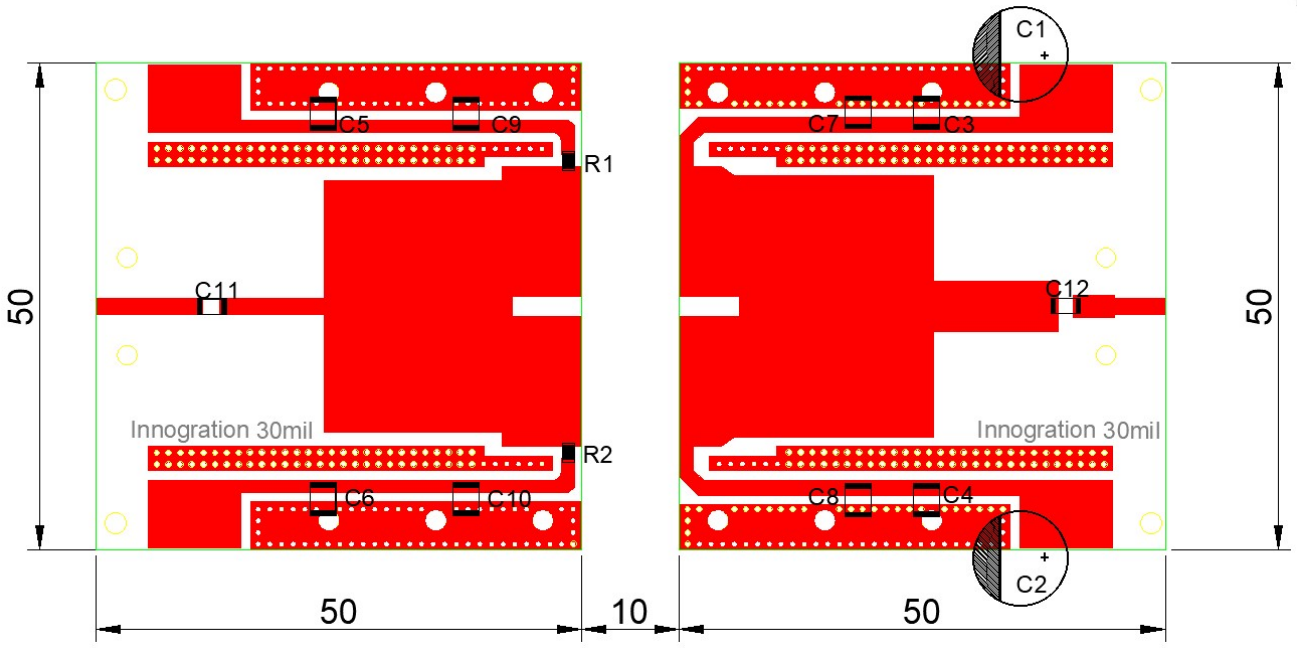
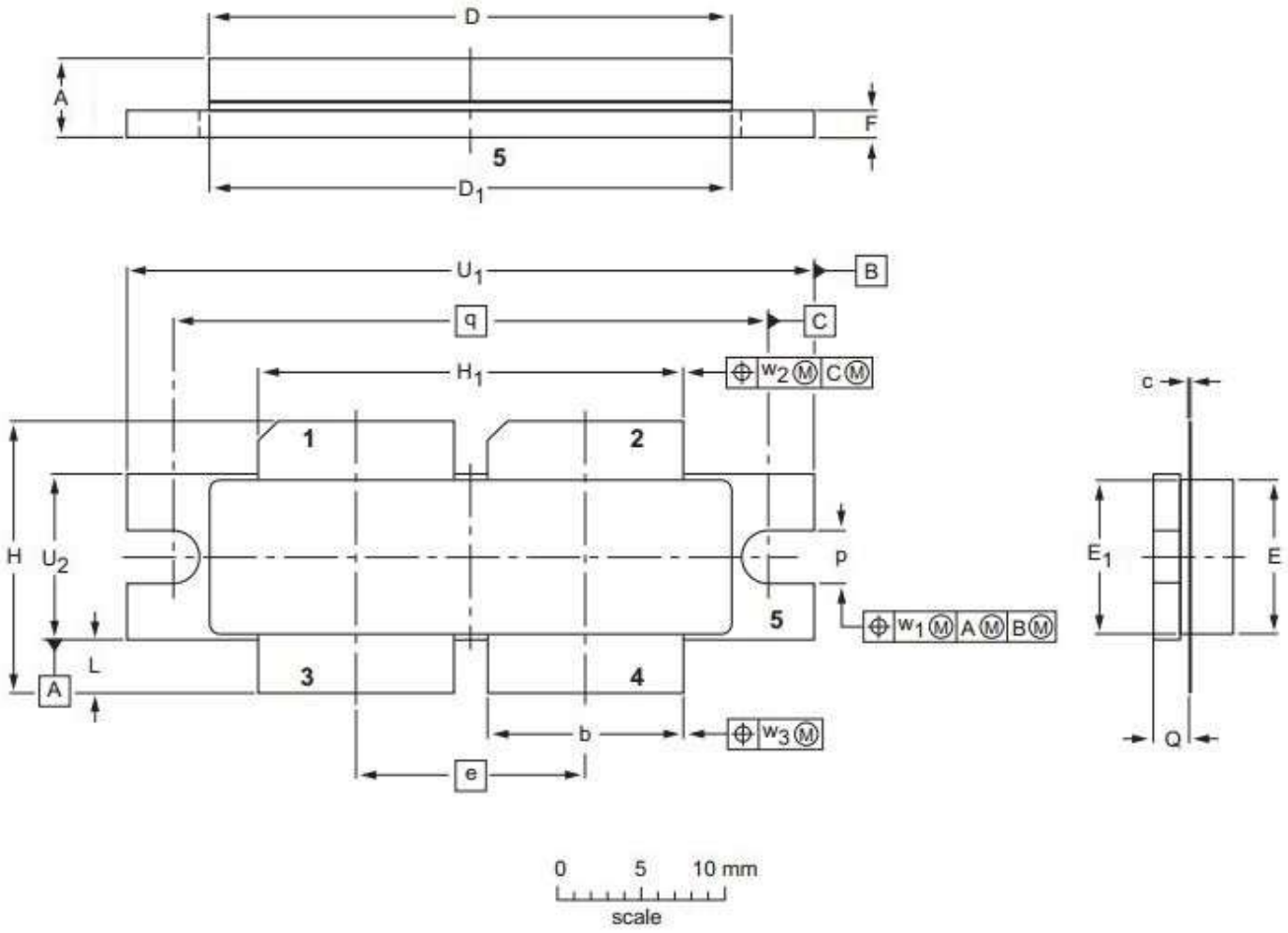


Figure 1. Test Circuit Component Layout

Component	Description	Suggestion
C1,C2	2200uF/63V	
C3,C4,C5,C6	10uF	1210
C7,C8,C9,C10,C11,C12	33pF	ATC 800B
R1,R2,	Chip Resistor,10Ω	0805
PCB	30 mil Rogers 4350B	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
Mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
Inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/12/2	Rev 1.0	Preliminary Datasheet Creation

Application data based on RXT-23-47

Disclaimers