Document Number: MQ161K0VP Preliminary Datasheet V1.0

1000W, 50V L band pulsed RF LDMOS FETs

Description

The MQ161K0VP is a 1000W, high performance, internally matched LDMOS FET,

designed for any applications with frequencies 1.3 to 1.6GHz.

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

Typical Pulse Performance (on innogration wide band test fixture with device soldered):
Vds = 50 V, Idq = 100 mA, TA = 25 °C, 1.3GHz

Pulsed CW conditions	Pin(dBm)	Pout(dBm)	Pout(W)	lds(A)	Gain(dB)	Eff(%)
8us,5%	49.54	61.32	1355	2.6	11.8	52
20us,20%	48.61	60.38	1100	8.6	11.8	51

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbo	bl	١	/alue		Unit	
DrainSource Voltage	V _{DSS}		115				
GateSource Voltage	V_{GS}		-10) to +10		Vdc	
Operating Voltage	V _{DD}			+55		Vdc	
Storage Temperature Range	Tstg		-65	to +150		°C	
Case Operating Temperature	Tc			+150		°C	
Operating Junction Temperature	TJ			+225		°C	
Table 2. Thermal Characteristics	•						
Characteristic	Symbo	ibol Value				Unit	
Thermal Resistance, Junction to Case, Case Temperature							
80°C, 1000W Pout, Pulse width: 8us, duty cycle: 5%,	Rejc		0.02			°C/W	
Vds=50 V, IDQ = 100 mA							
Table 3. ESD Protection Characteristics	-						
Test Methodology				Class			
Human Body Model (per JESD22A114)		Class 2					
Table 4. Electrical Characteristics (TA = 25 °C unless other the state of the state	herwise note	d)					
Characteristic		Symbol	Min	Тур	Max	Unit	
DC Characteristics	L.				1		
Drain-Source Breakdown Voltage		V _{DSS}	115			V	



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(V _{GS} =0V; I _D =100uA)					
Zero Gate Voltage Drain Leakage Current			10		
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}		10	μA	
GateSource Leakage Current	1		1		
$(V_{GS} = 6 V, V_{DS} = 0 V)$	IGSS		I	μΑ	
Gate Threshold Voltage	V (th)	1.6		v	
(V _{DS} = 50V, I _D = 600 uA)	V _{GS} (th)	1.0		v	
Gate Quiescent Voltage	V _{GS(Q)}	3		V	
(V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	V GS(Q)	3		V	

Reference Circuit of Test Fixture (Layout file upon request) PCB: Roger 4350B, 20mils

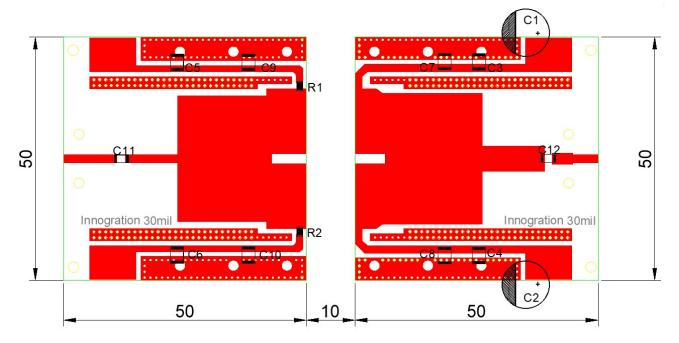
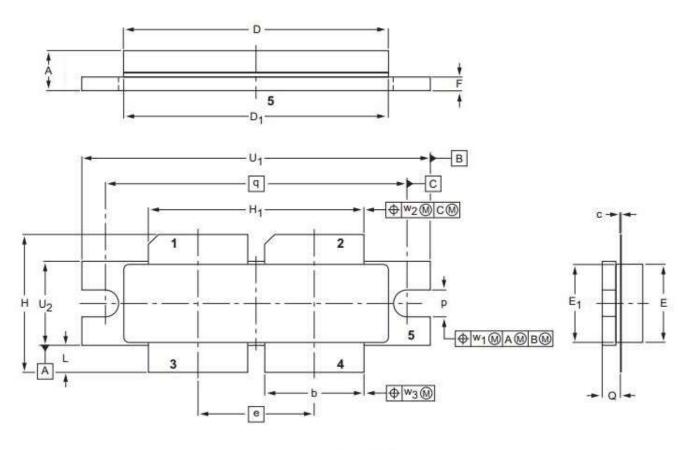


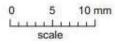
Figure 1. Test Circuit Component Layout

Component	Description	Suggestion
C1,C2	2200uF/63V	
C3,C4,C5,C6	10uF	1210
C7,C8,C9,C10,C11,C12	33pF	ATC 800B
R1,R2,	Chip Resistor,10Ω	0805
РСВ	30 mil Rogers 4350B	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1, 2-DRAIN, 3, 4-GATE, 5-SOURCE)





U	літ	A	b	с	D	D1	е	Е	E1	F	н	H1	L	р	Q	q	U1	U ₂	W1	W ₂	W ₂
	Im	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	IIII	4.2	11.56	0.10	30.94	30.96	13.72	9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03		0.31	0.25
	h	0.185	0.185 0.465 0.007 1.2	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01	
inc	hes	0.165	0.455	0.004	1.218	1.219	0.340	0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079	1.400	1.615	0.395	0.01	0.02	0.01

OUTLINE		REFERENCE		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	1000E DATE
PKG-D4E				$\bigcirc \bigcirc$	03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/12/2	Rev 1.0	Preliminary Datasheet Creation

Application data based on RXT-23-47

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