10W,28V Plastic RF LDMOS Transistor

ITEH27010P3

Description

The ITEH27010P3 is a 10-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2.7GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

•Typical 1.8GHz Class AB RF Performance (On Innogration fixture with device soldered).

VDS=**28V**, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1810	40.78	12.0	58.3	20.26	41.53	14.2	60
1850	40.28	10.7	57.7	20.7	41.24	13.3	60
1880	39.83	9.6	56.4	20.32	41.04	12.7	60

•Typical 2.1GHz Class AB RF Performance (On Innogration fixture with device soldered).

VDS=**28V**, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2110	41.06	12.8	54.8	17.09	42	15.9	58.0
2140	40.58	11.4	56.7	17.04	41.54	14.3	59.1
2170	39.98	10.0	55.8	16.86	41	12.6	57.8

•Typical 2.6GHz Class AB RF Performance (On Innogration fixture with device soldered).

VDS=**28V**, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2600	41.13	12.97	52.00	15.87	41.99	15.80	54.53
2650	40.72	11.80	51.59	16.09	41.86	15.35	55.78
2700	40.39	10.95	50.50	15.61	41.63	14.55	54.90

Note: High linear tuning result for each band upon request

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Broadcast and Industrial, Scientific and Medical applications in the frequency range from HF to 2.7GHz
- All 4G/5G cellular application below 2.7GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc

Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=10W 2.1GHz	RθJC	1.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

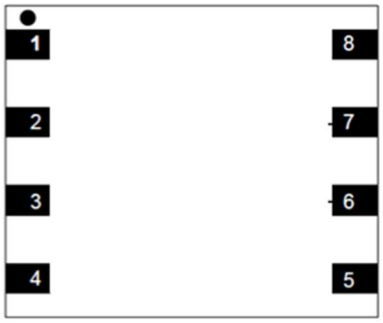
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.8	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 2100 MHz

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

2500-2700MHz

Reference Circuit of Test Fixture Assembly Diagram

RO4350B 20mils

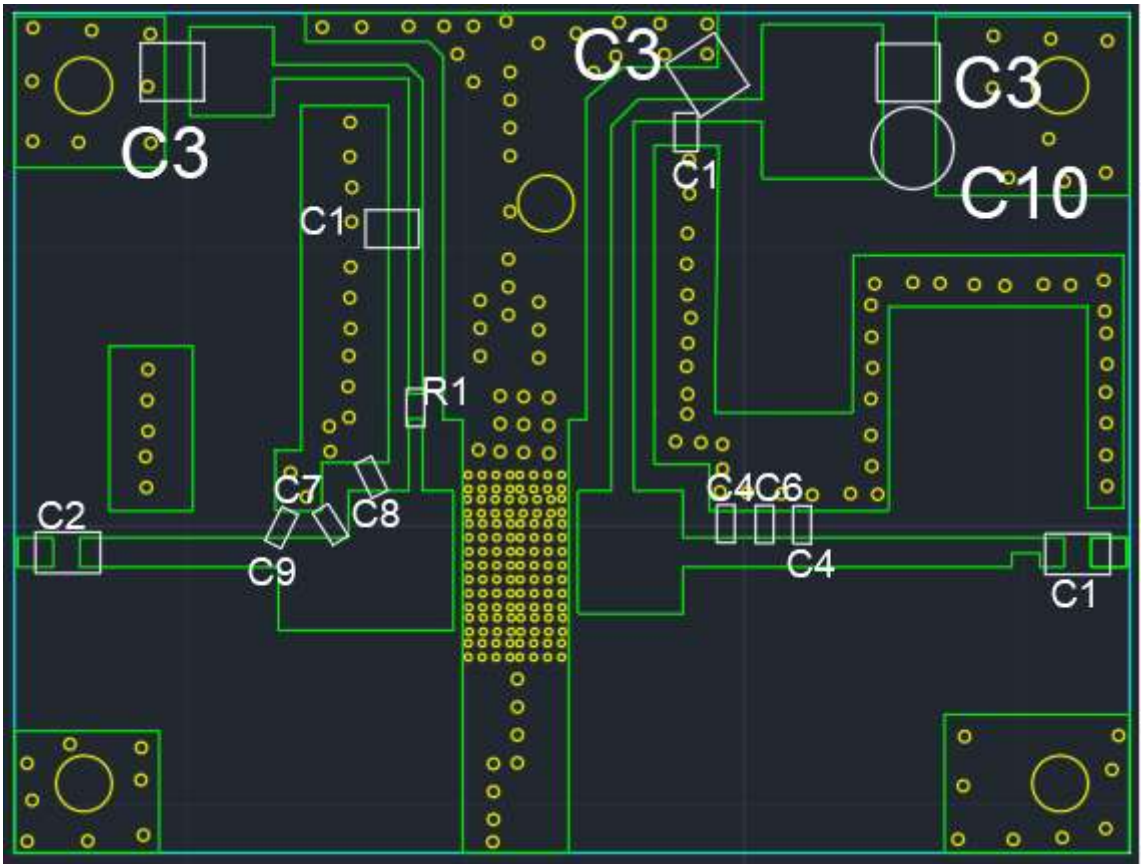


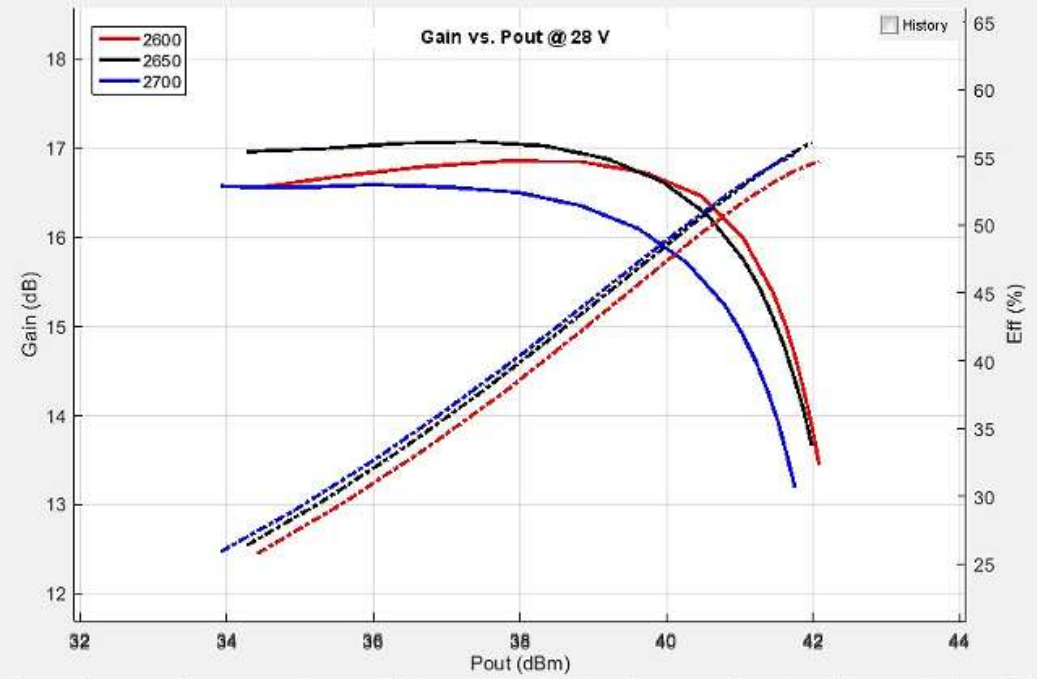
Figure 2. Test Circuit Component Layout

Table 4. Test Circuit Component Designations and Values

BOM		
Component	**Value**	**Quantity**
C2	3.9pF	1
C3	10uF/63V	3
R1	10 ohm	1
C1	12pF	3
C4	0.1pF	2
C10	470uF	1
C6	2.2 pF	1
C7	1.6pF	1
C8	2pF	1
C9	0.3pF	1

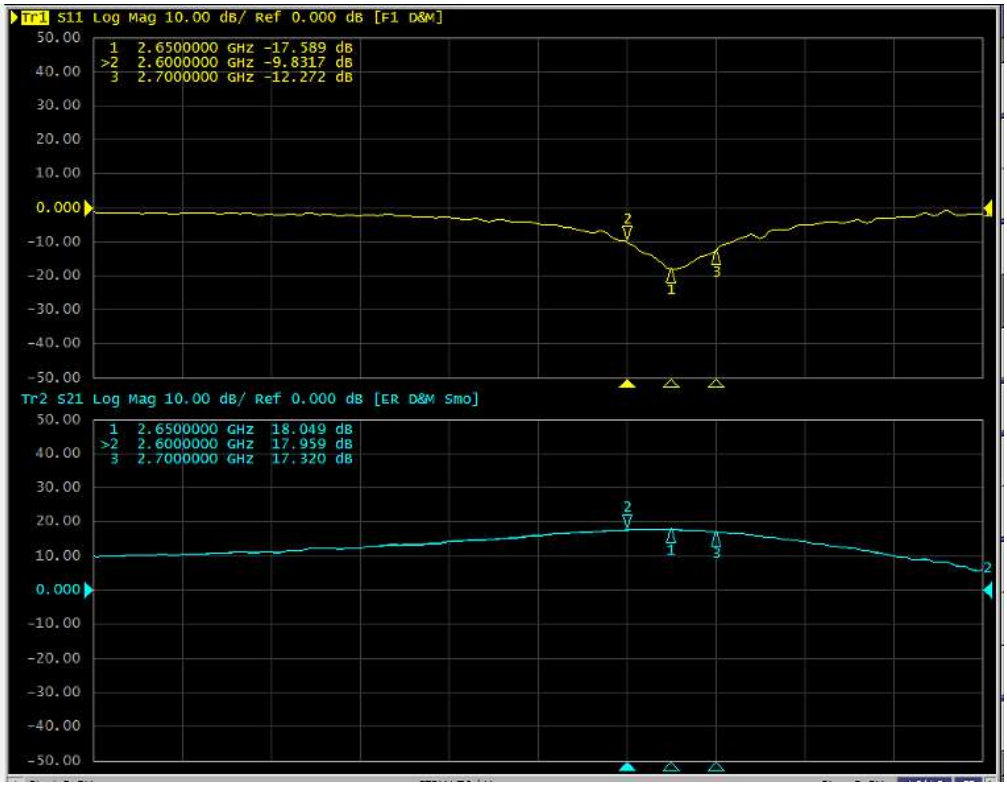
TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Out



	Freq(MHz)	PX1dB(dBm)	PX1dB(W)	PX1dB Eff(%)	PX1dB Gain(dB)	PX2dB(dBm)	PX2dB(W)	PX2dB Eff(%)	No
1	Freq(MHz)	P1dB(dBm)	P1dB(W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB(dBm)	P3dB(W)	P3dB Eff(%)	CW-67
2	2600.0	41.13	12.97	52.00	15.87	41.99	15.80	54.53	
3	2650.0	40.72	11.80	51.59	16.09	41.86	15.35	55.78	
4	2700.0	40.39	10.95	50.50	15.61	41.63	14.55	54.90	

Figure 4.Network analyzer output S11/S21



2110-2170MHz

Reference Circuit of Test Fixture Assembly Diagram

RO4350B 20mils

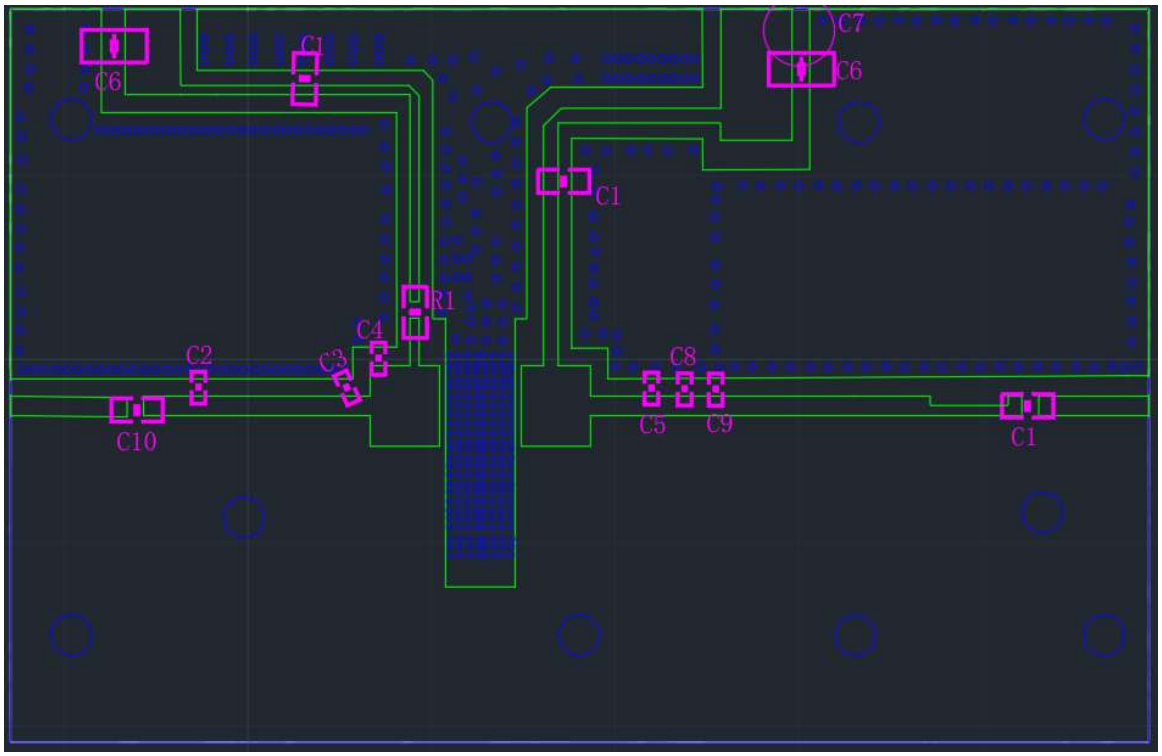


Figure 5. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

BOM		
Component	Value	Quantity
C2	1.2pF	1
C3	3.9pF	3
R1	10 ohm	1
C1	20pF	3
C4	2.4pF	1
C9	0.2 pF	1
C5	0.3 pF	1
C6	10uF/63V	1
C7	470uF	1
C8	2pF	1
C10	6.8pF	1

TYPICAL CHARACTERISTICS

Figure 6. Power Gain and Drain Efficiency as function of Power Out

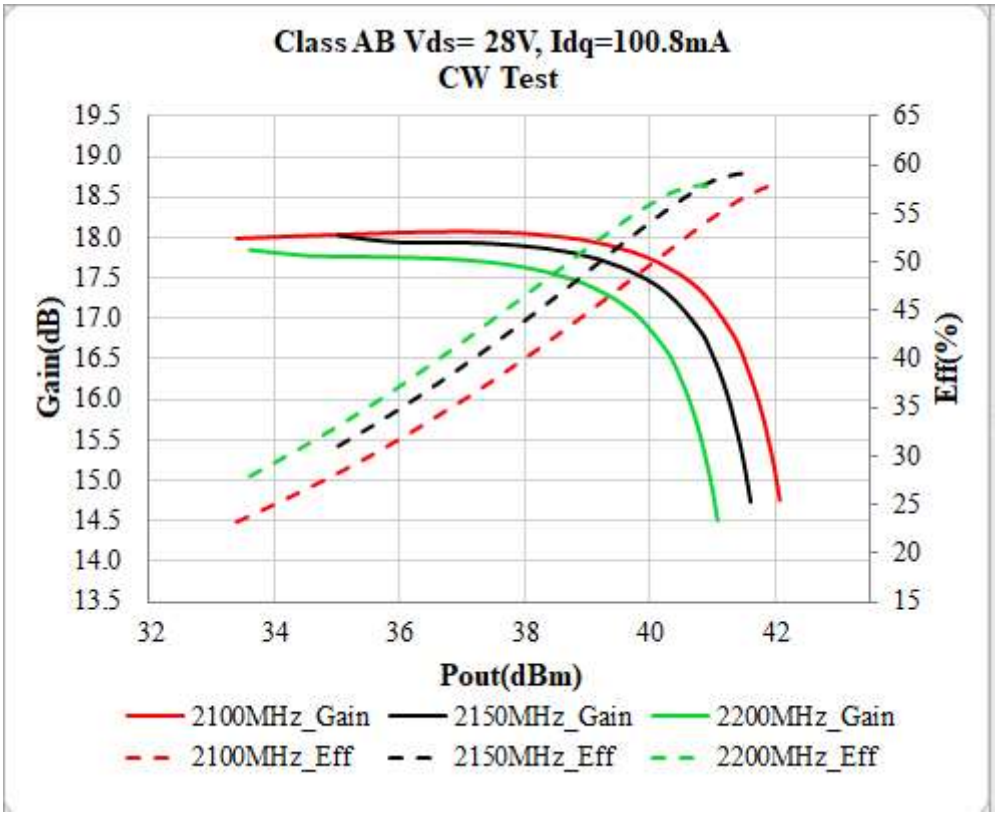
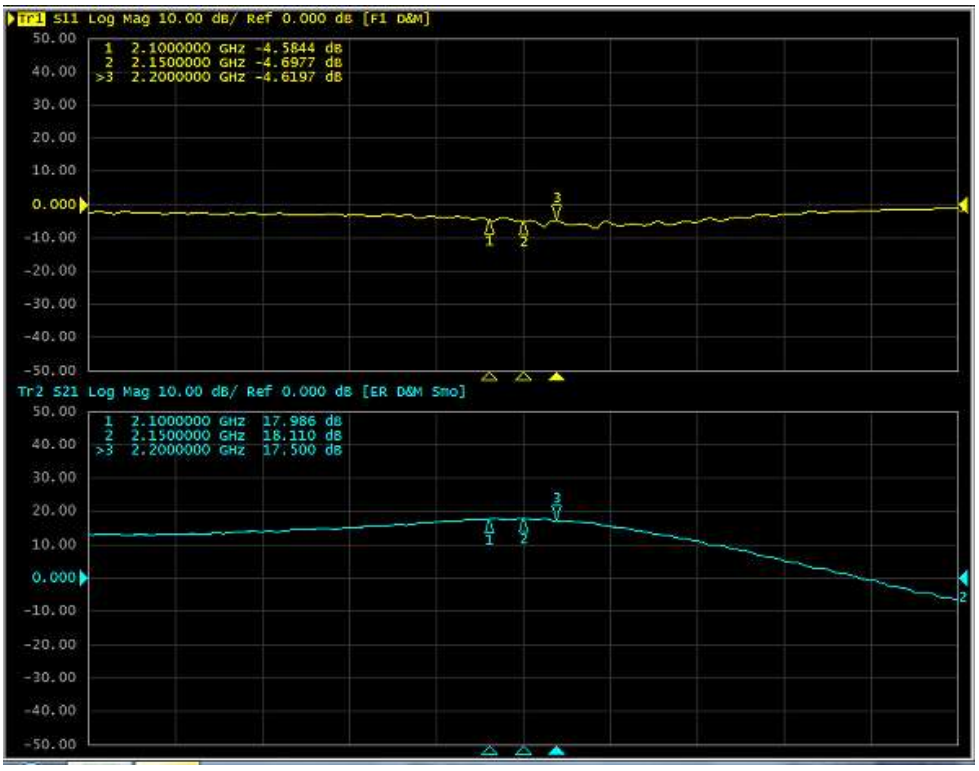


Figure 7.Network analyzer output S11/S21



1810-1880MHz

Reference Circuit of Test Fixture Assembly Diagram

RO4350B 20mils

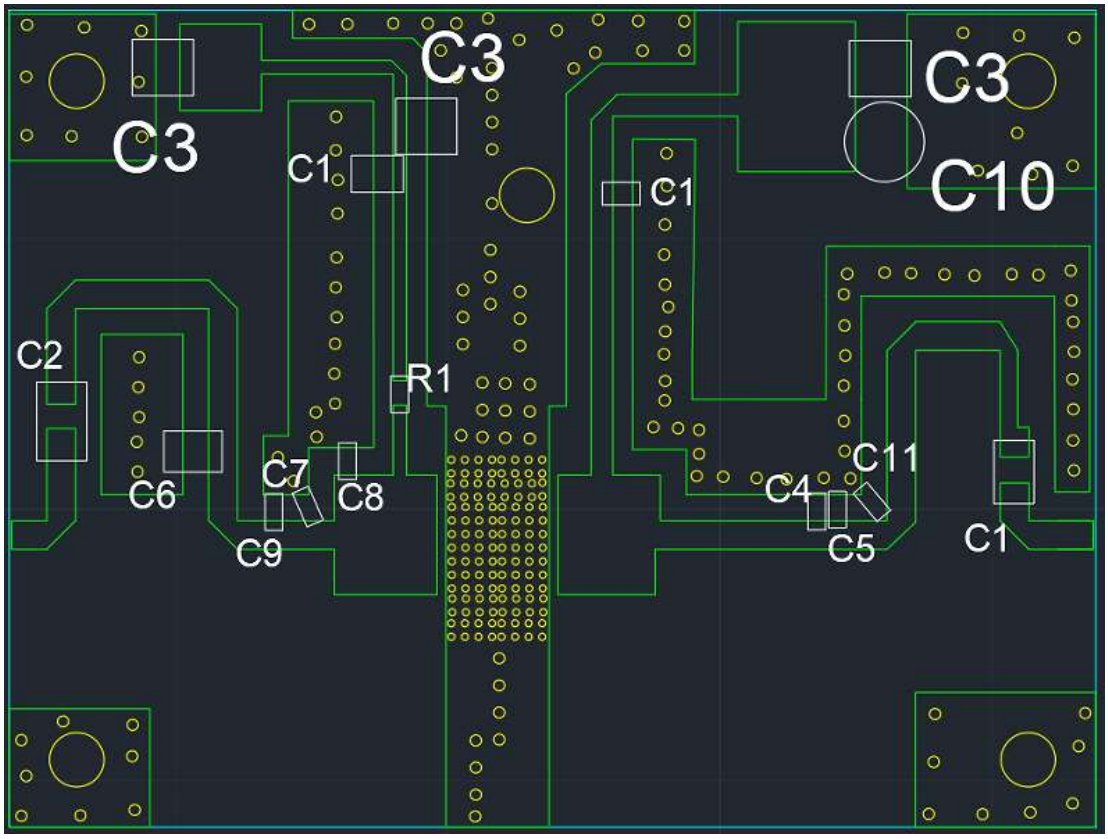


Figure 8. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

BOM		
Component	**Value**	**Quantity**
C2	3.9pF	1
C3	10uF/63V	3
R1	10 ohm	1
C1	20pF	3
C4	2.2pF	1
C10	470uF	1
C5	0.5 pF	1
C6	1 pF	1
C7	3.9pF	1
C8	2pF	1
C9	0.1pF	1
C11	1.1pF	1

TYPICAL CHARACTERISTICS

Figure 9. Power Gain and Drain Efficiency as function of Power Out

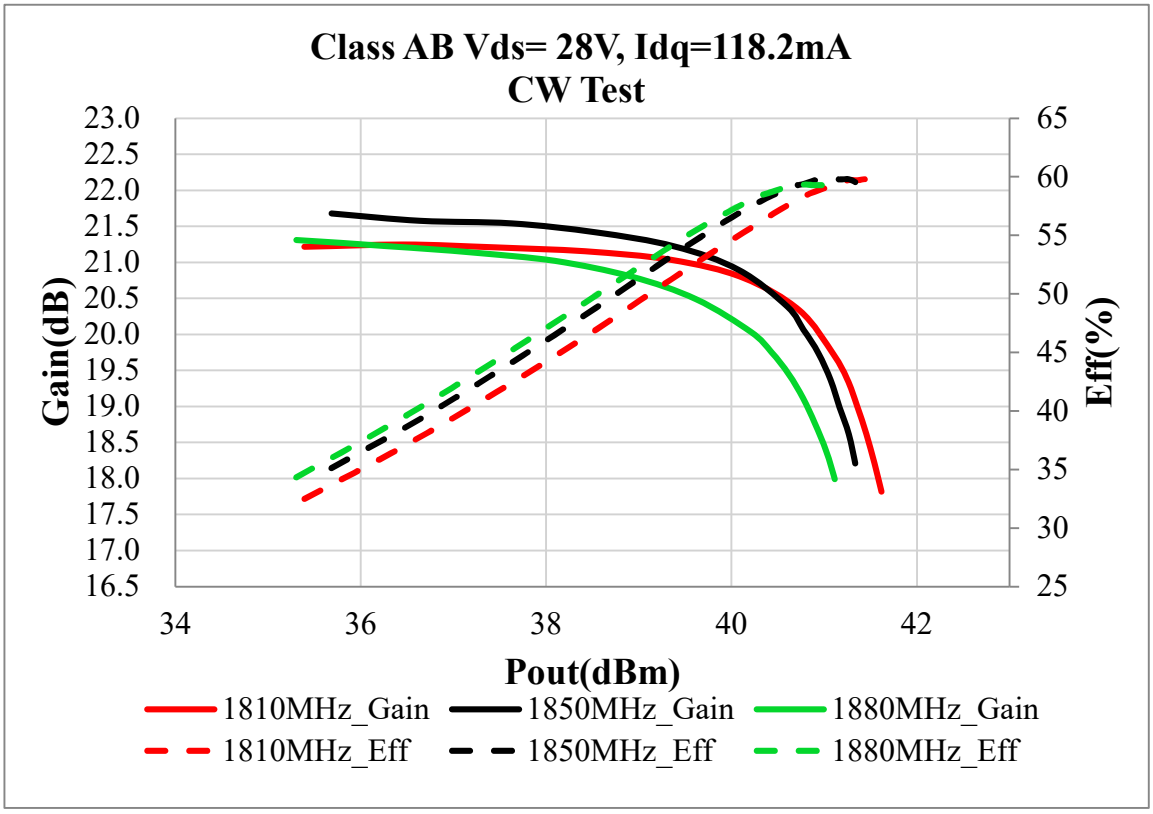
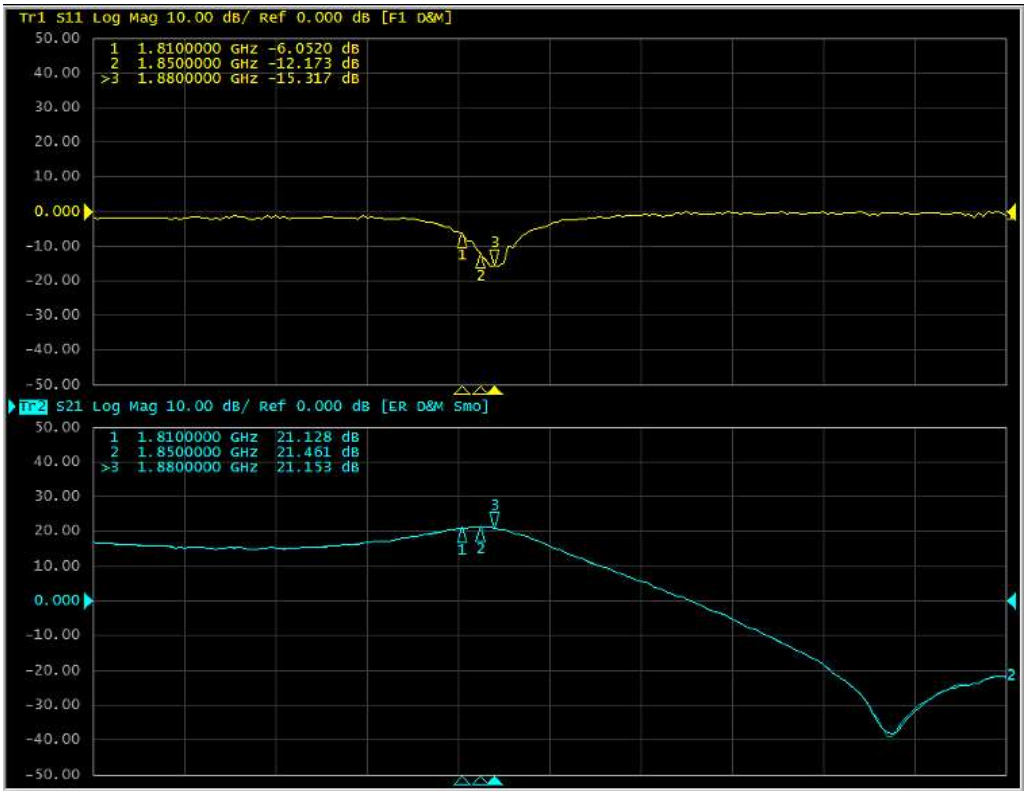
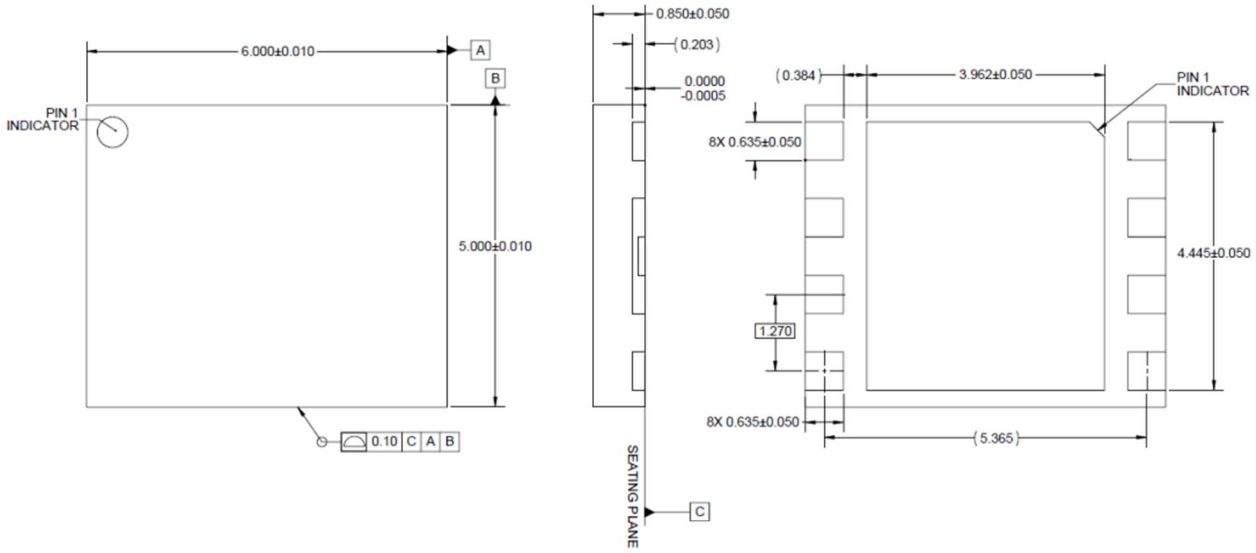


Figure 10.Network analyzer output S11/S21



Package

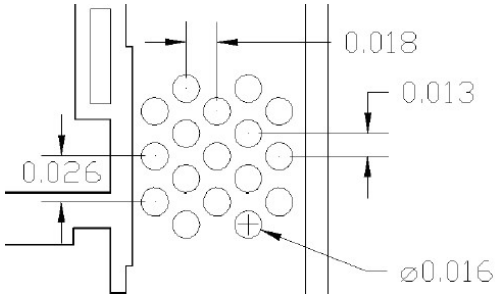
6*5 DFN Package



Notes:

1. All dimensions are in mm. Otherwise noted, the tolerance is ±0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/12/14	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-23-16/17/18

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