



7W,28V Plastic RF LDMOS Transistor

ITEH38007P3



Description

The ITEH38007P3 is a 7-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 3.8GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

- Typical 3.3-3.6GHz Class AB RF Performance (On Innegration fixture with device soldered).

WCDMA 1 carrier PAR=10.8dB

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
3300	28.81	9.73	-46.0	14.0	14.2
3400	28.79	9.91	-46.8	15.1	15.8
3500	28.79	9.62	-46.0	15.3	16.6
3600	28.81	9.40	-46.3	14.2	16.2

- Typical 2.5-2.7GHz Class AB RF Performance (On Innegration fixture with device soldered).

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2500	28.81	10.02	-47.39	16.44	16.71
2600	28.77	9.90	-47.75	16.98	18.47
2700	28.79	9.64	-47.22	16.41	19.72

- Typical 2.1-2.2GHz Class AB RF Performance (On Innegration fixture with device soldered).

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2100	28.80	9.69	-48.1	17.4	18.0
2150	28.78	9.76	-47.5	17.4	19.0
2200	28.76	9.46	-47.0	16.6	19.7

- Typical 758-803MHz Class AB RF Performance (On Innegration fixture with device soldered).

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
758	28.76	9.81	-45	17.3	21.72
780	28.77	9.82	-45	17.07	22.05
803	28.81	9.66	-45	17.12	22.29

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Broadcast and Industrial, Scientific and Medical applications in the frequency range from HF to 3.8GHz
- All 4G/5G cellular application below 3.8GHz

Table 1. Maximum Ratings



Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $P_{out} = 7\text{W}$ 3.4GHz	$R_{\theta JC}$	2.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

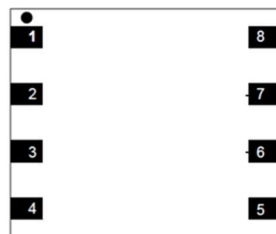
Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 100\mu\text{A}$	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_D = 70\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.8	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 70\text{mA}$, $f = 2100\text{MHz}$

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation
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Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /MDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

3300-3600MHz
Reference Circuit of Test Fixture Assembly Diagram
RO4350B 20mils

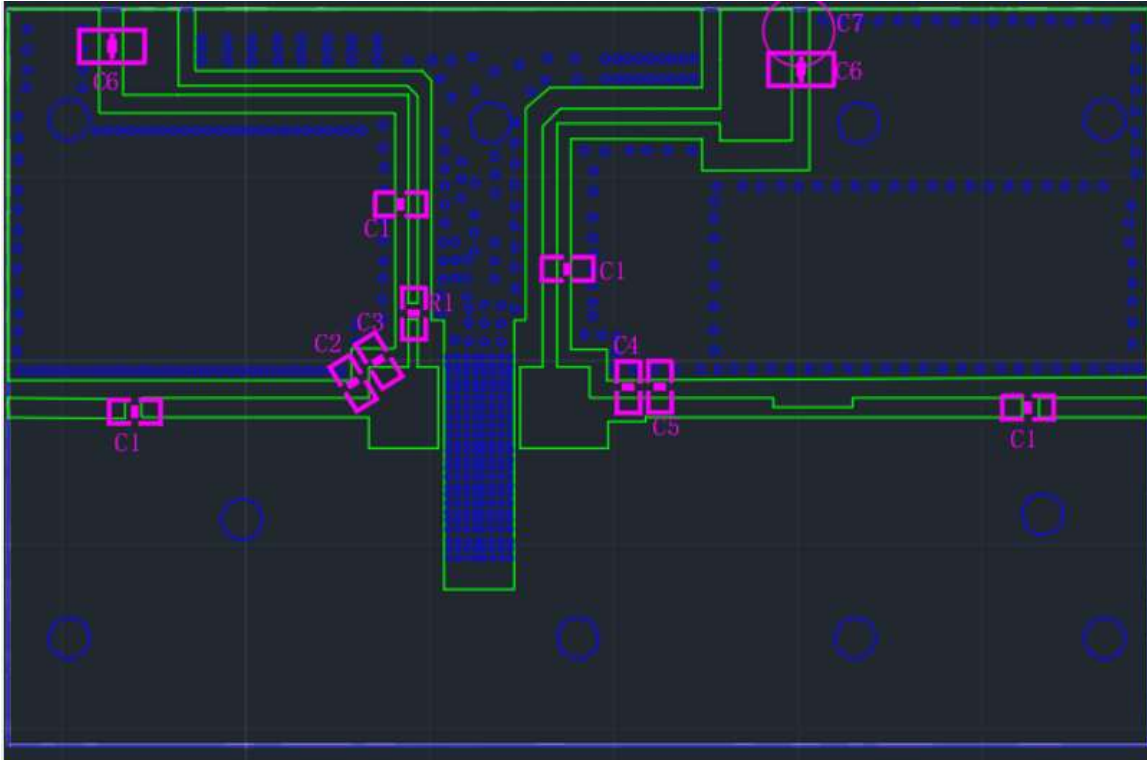


Figure 2. Test Circuit Component Layout

Table 4. Test Circuit Component Designations and Values

BOM		
Component	Value	Quantity
C6	10uF/63V	2
R1	10 ohm	1
C1	8.2pF	4
C4	1.2pF	1
C7	470uF	1
C2	0.3 pF	1
C3	1.2pF	1
C5	0.1pF	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Out

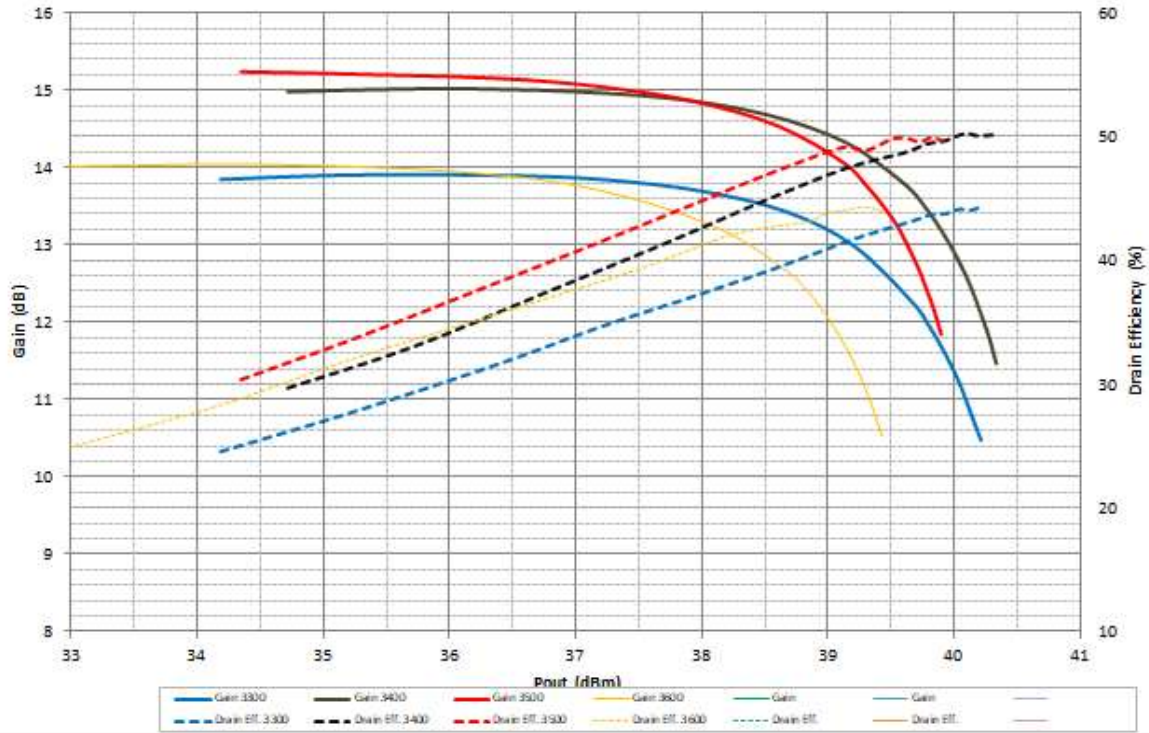
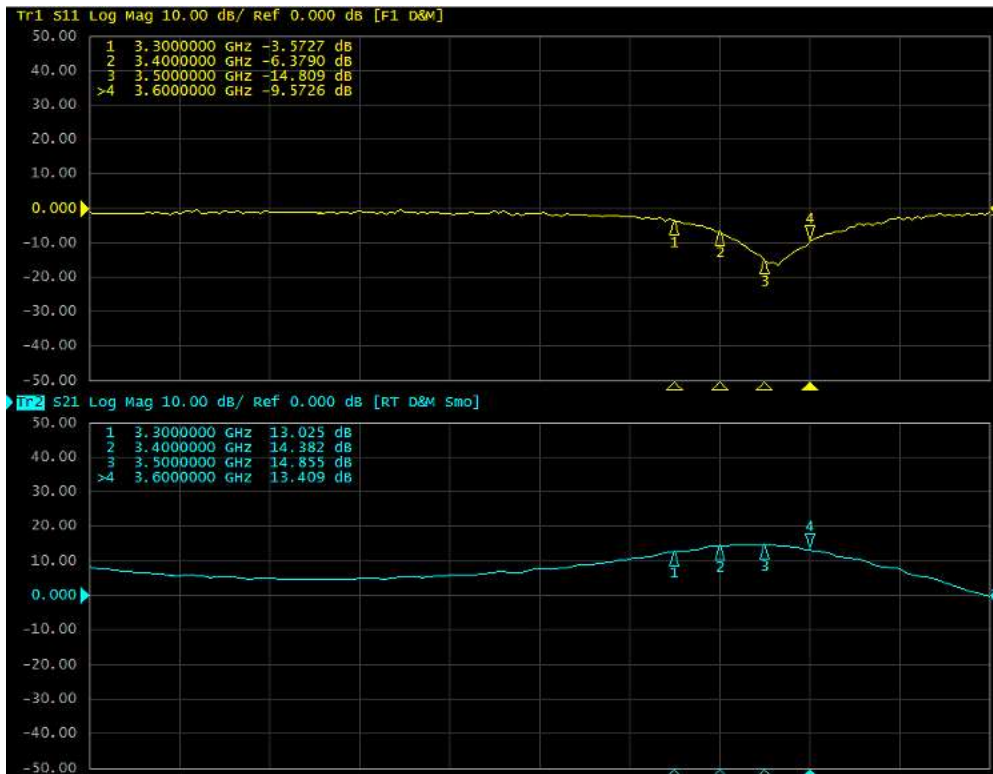


Figure 4. Network analyzer output S11/S21



2500-2700MHz
Reference Circuit of Test Fixture Assembly Diagram
RO4350B 20mils

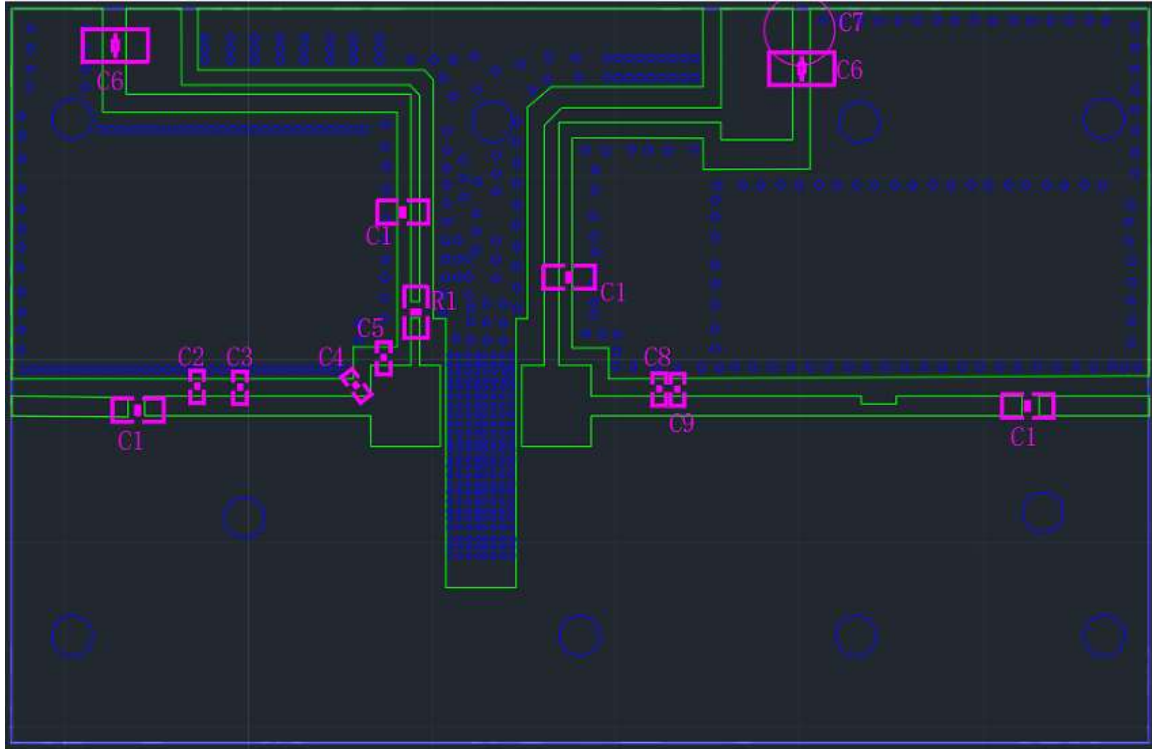


Figure 5. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

BOM		
Component	Value	Quantity
C6	10uF/63V	2
R1	10 ohm	1
C1	12pF	4
C2	0.3pF	1
C7	470uF	1
C3	1.2pF	1
C4	2pF	1
C5	2pF	1
C8	1 pF	1
C9	1.2 pF	1

TYPICAL CHARACTERISTICS

Figure 6. Power Gain and Drain Efficiency as function of Power Out

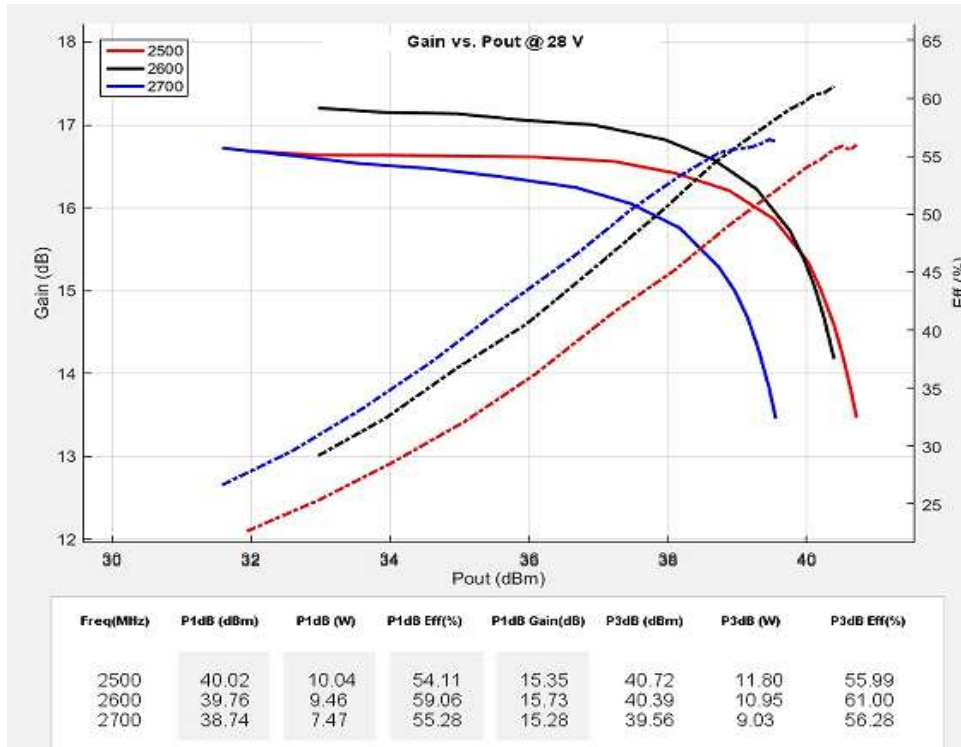
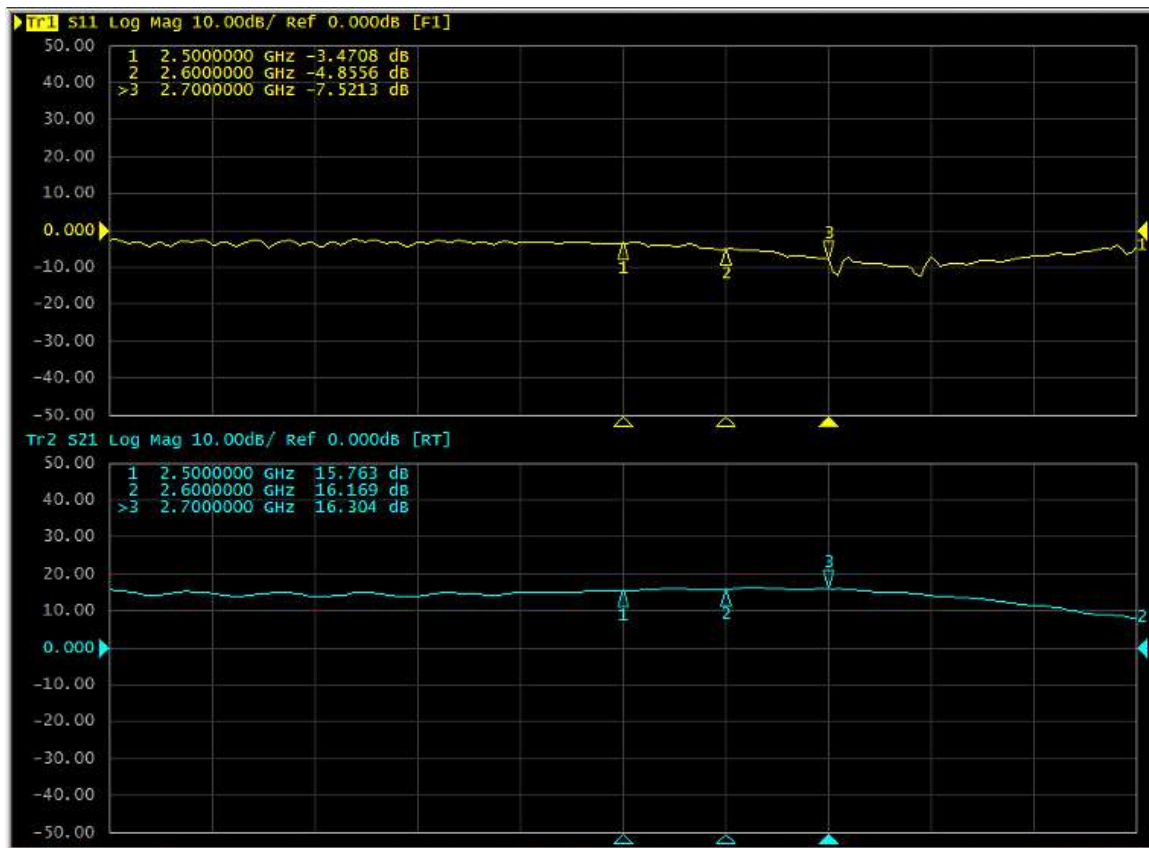


Figure 7. Network analyzer output S11/S21



2100-2200MHz
Reference Circuit of Test Fixture Assembly Diagram
RO4350B 20mils

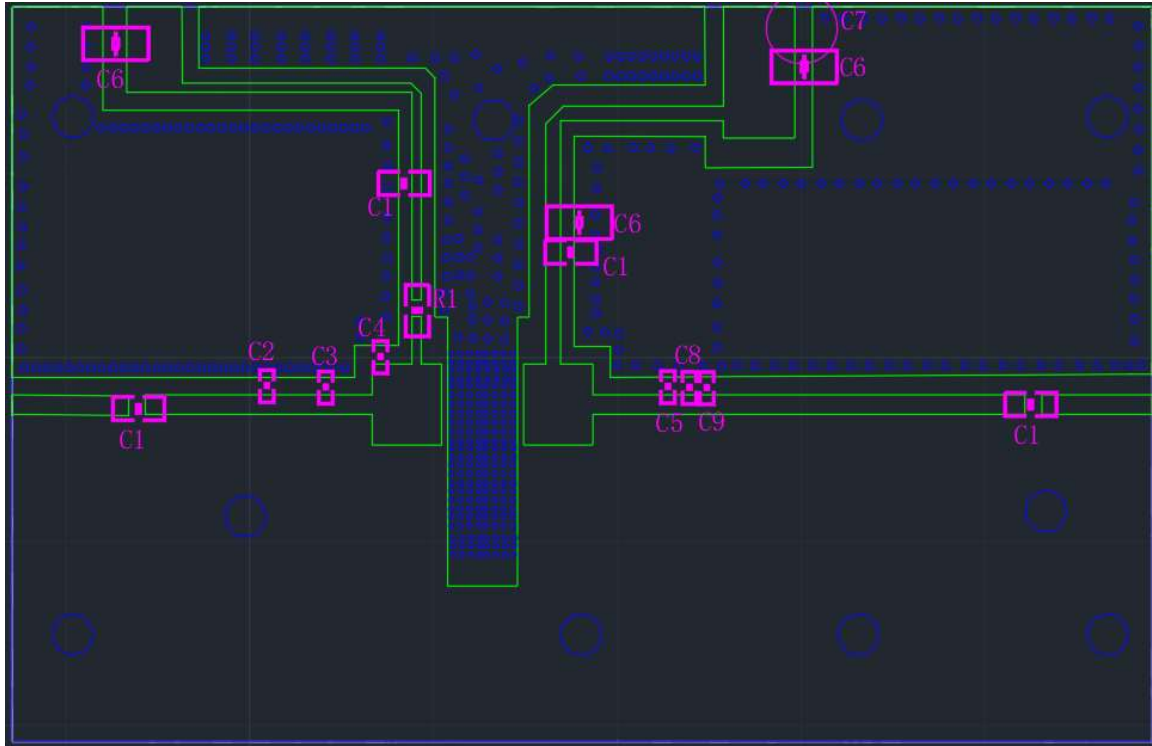


Figure 8. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Component	BOM	
	Value	Quantity
C6	10uF/63V	2
R1	10 ohm	1
C1	20pF	4
C4	2.2pF	1
C7	470uF	1
C2	1.8 pF	1
C3	0.7pF	1
C5	0.1pF	1
C8	0.4 pF	1
C9	2 pF	1

TYPICAL CHARACTERISTICS

Figure 9. Power Gain and Drain Efficiency as function of Power Out

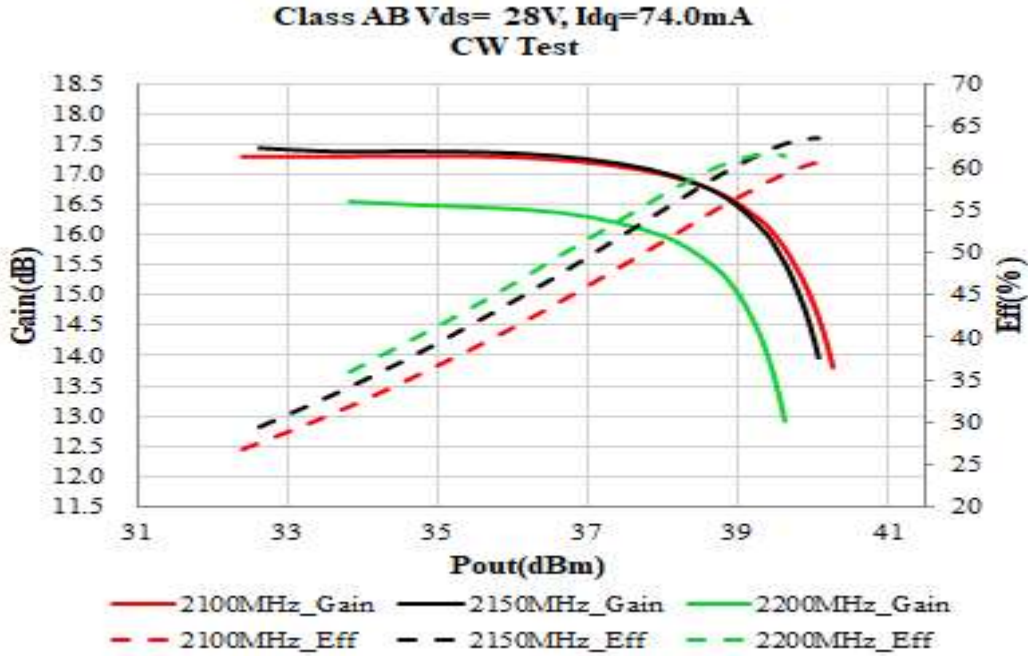


Figure 10. Network analyzer output S11/S21



758-803MHz
Reference Circuit of Test Fixture Assembly Diagram
RO4350B 20mils

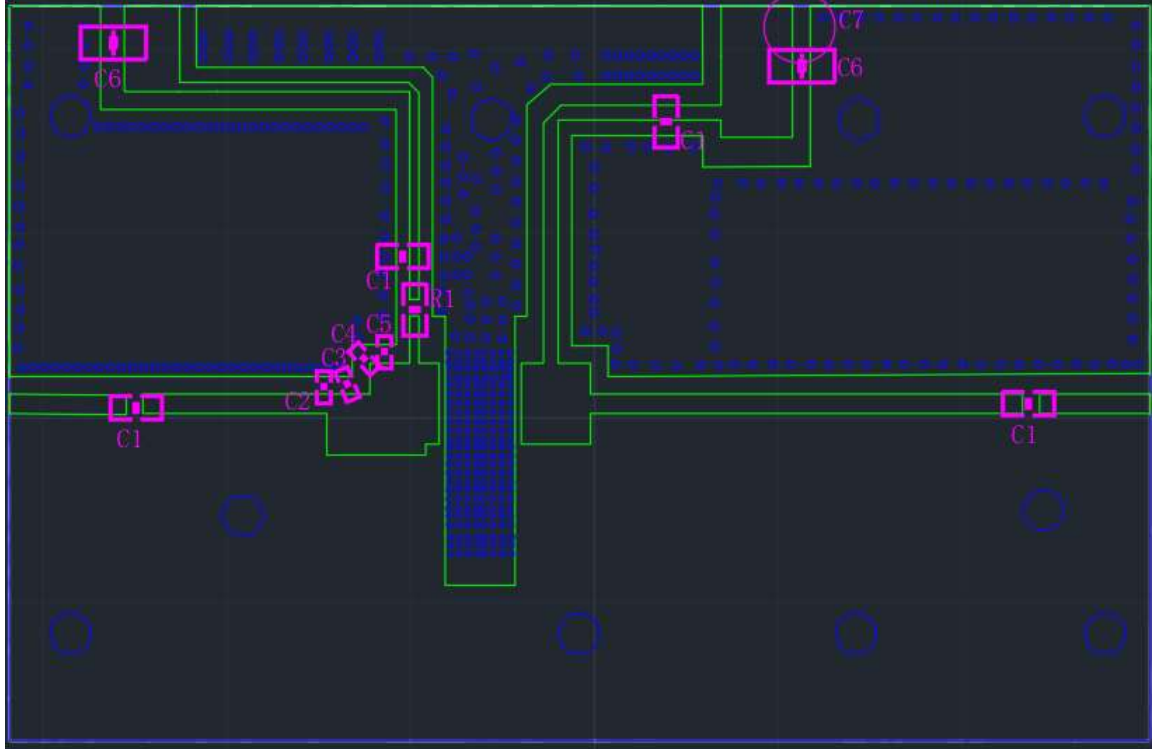


Figure 11. Test Circuit Component Layout

Table 7. Test Circuit Component Designations and Values

Component	BOM	
	Value	Quantity
C6	10uF/63V	2
R1	10 ohm	1
C1	100pF	4
C4	2pF	1
C7	470uF	1
C2	2.7 pF	1
C3	2.7pF	1
C5	2.7pF	1

TYPICAL CHARACTERISTICS

Figure 12. Power Gain and Drain Efficiency as function of Power Out

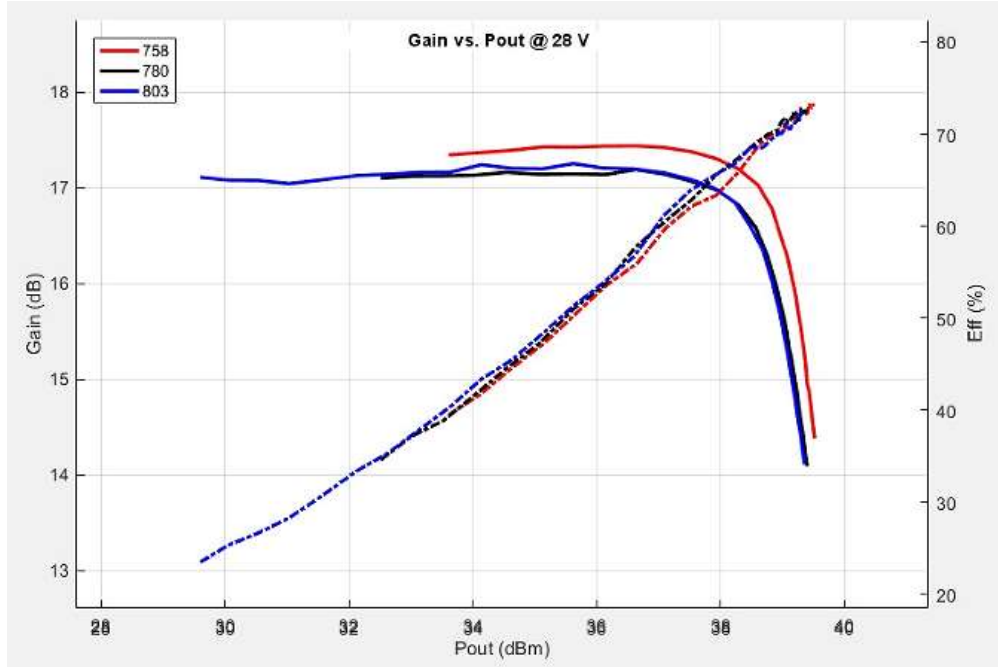


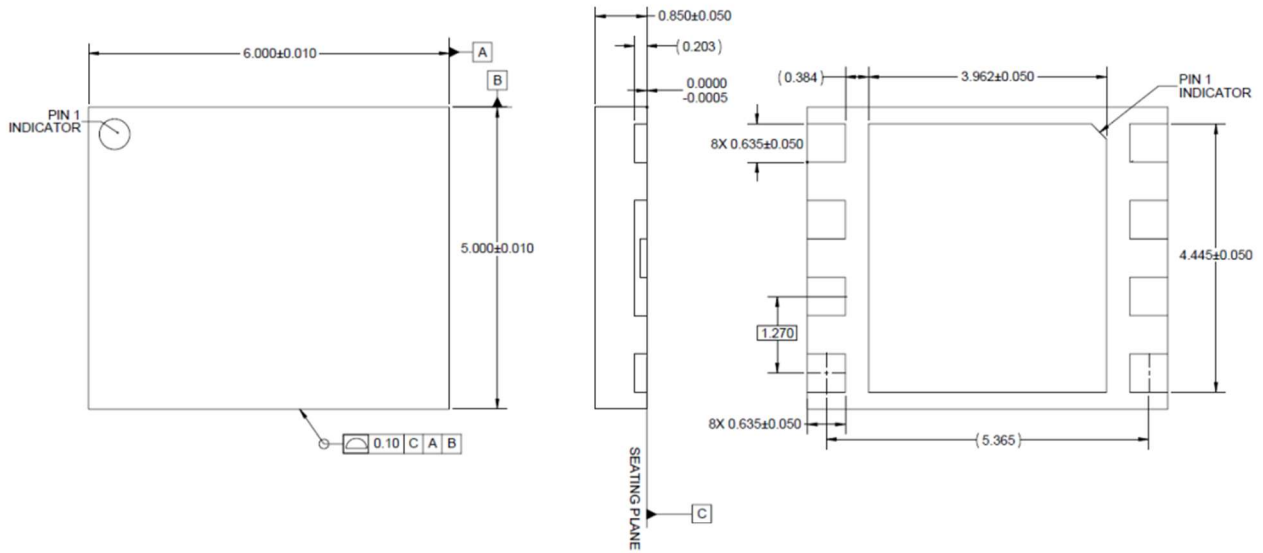
Figure 13. Network analyzer output S11/S21





Package

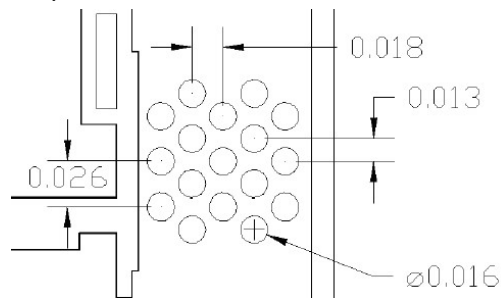
6*5 DFN Package



Notes:

1. All dimensions are in mm. Otherwise noted, the tolerance is ± 0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)





Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/12/21	Rev 1.0	Preliminary Datasheet
2024/1/2	Rev 1.1	Add 2.1G application data

Application data based on ZXY-23-21/23/24, 24-01

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