

MV0530VX LDMOS TRANSISTOR

Document Number: MV0530VX
Preliminary Datasheet V3.0

300W, HF-0.5GHz 50V High Power RF LDMOS

Description

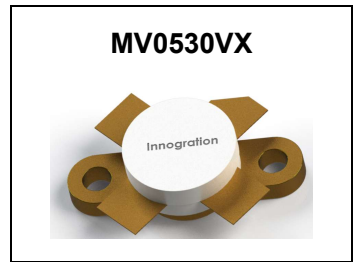
The MV0530VX is a 300W single ended 50V LDMOS, unmatched for any applications within HF-0.5GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It can be the drop-in replacement of its equivalent 300W single ended VDMOS like SD2933/VRF2933 with improved RF performance like higher efficiency

- Typical performance(on Innogration test board with device soldered)

Signal: CW , $V_{gs}=3.35v, V_{ds}=50v, I_{dq}=200mA$



Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	I _{ds} (A)	Gain(dB)	Eff(%)	2 nd Harmonic(dB)	3 rd Harmonic(dB)
30	33.2	55.6	350	9.5	24	74	-27	-39

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^\circ C, T_j=200^\circ C, DC\ test$	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

MV0530VX LDMOS TRANSISTOR

Document Number: MV0530VX
Preliminary Datasheet V3.0

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10V, V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50V, I_D = 600 \mu A$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 50V, I_D = 200mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.4	—	V
Drain source on state resistance ($V_{ds}=0.1V, V_{gs}=10V$)	$R_{ds(on)}$		180		$m\Omega$
Common Source Input Capacitance ($V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$)	C_{iss}		220		pF
Common Source Output Capacitance ($V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$)	C_{oss}		65		pF
Common Source Feedback Capacitance ($V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$)	C_{rss}		1.5		pF
Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50Vdc, I_{DQ} = 200mA, f = 108MHz$, pulse width:100us, duty cycle:10%					
Load 20:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation				

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 30MHz

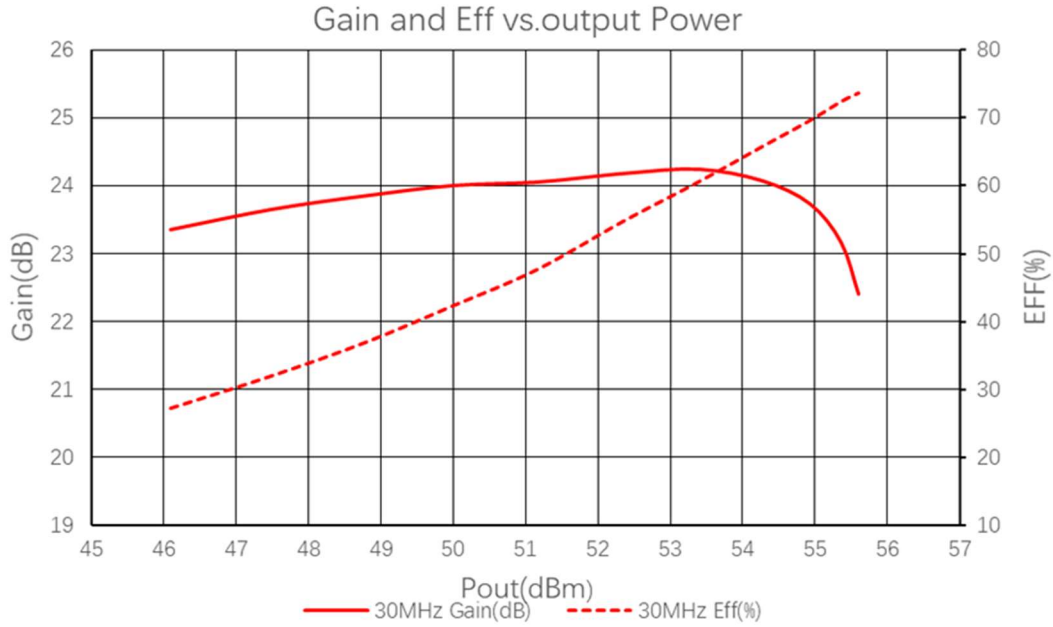


Figure 1: Network analyzer output S11/221



MV0530VX LDMOS TRANSISTOR

Document Number: MV0530VX
Preliminary Datasheet V3.0

Reference Circuit of Test Fixture Assembly Diagram (PCB file upon request)

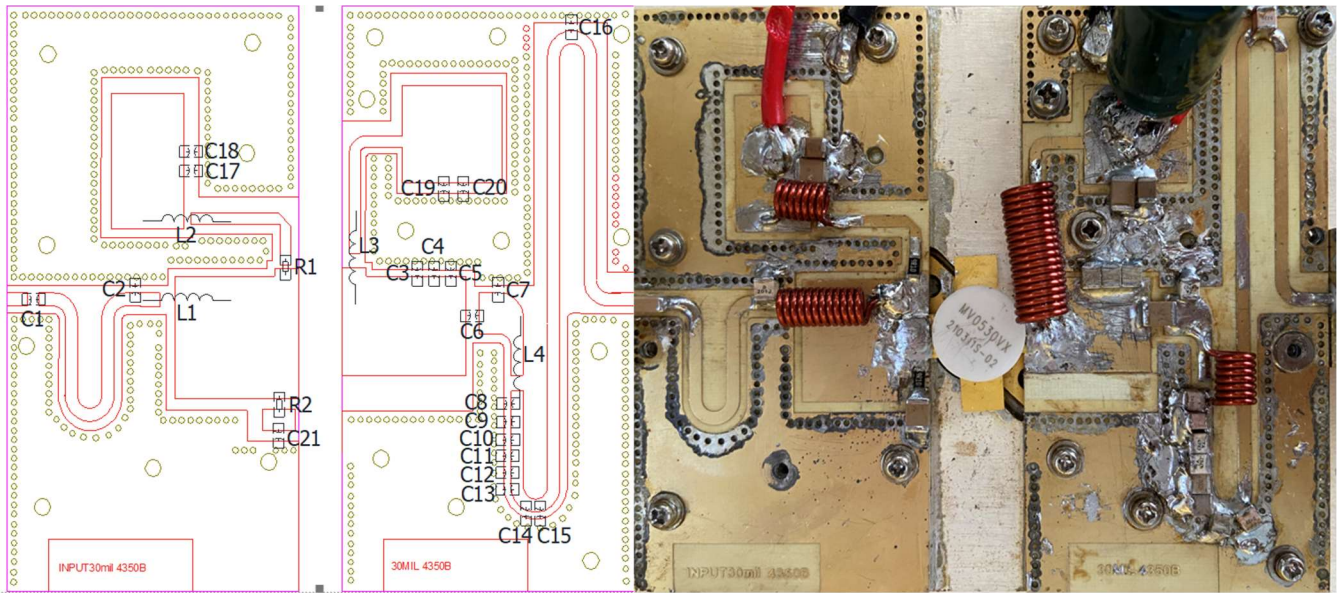


Table 1. Test Circuit Component Designations and Values (30MHz)

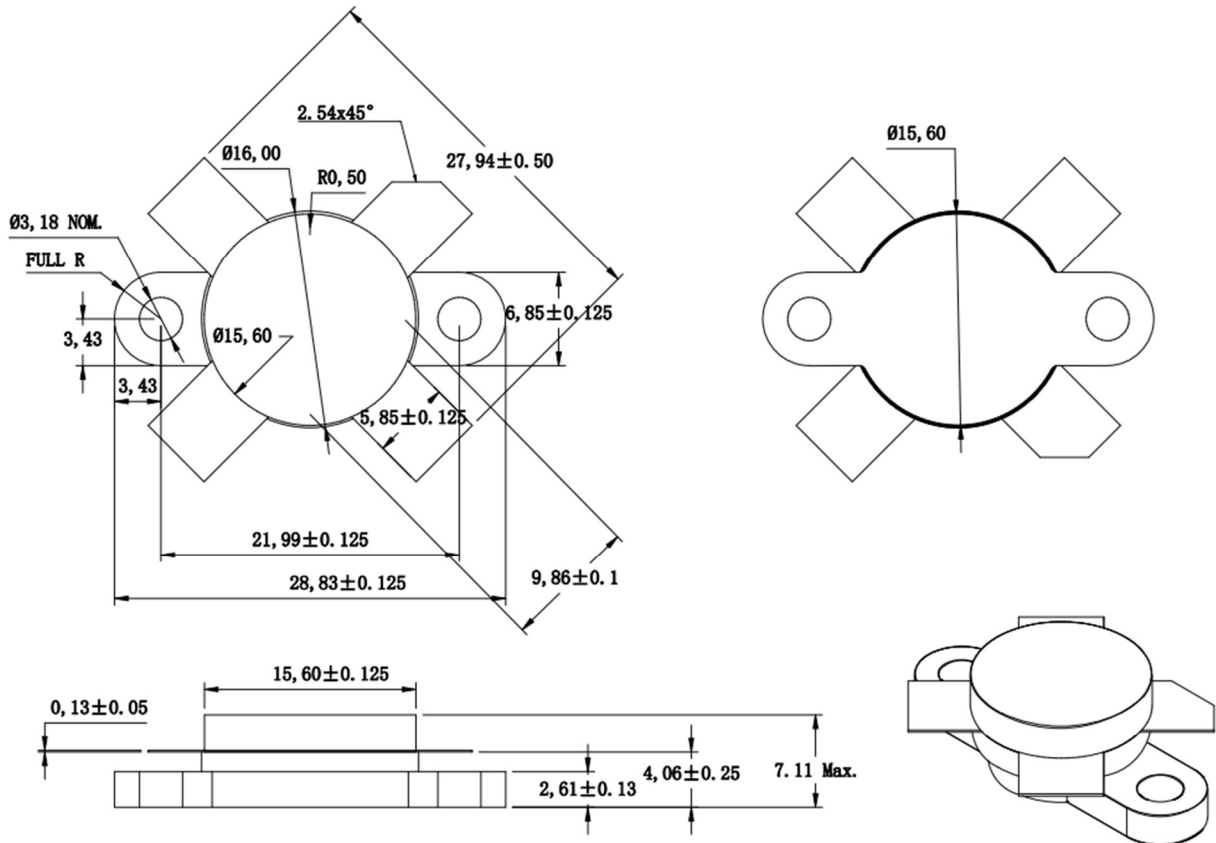
Component	Description	Suggestion
C1,C6,C17,C19,C21	10nF	CC1812KKX7RDBB103
C2	200pF	ATC800B
C3,C4,C14	68pF	ATC800B
C5,C12	100pF	ATC800B
C7,C10,C11,C13	47pF	DLC70B
C8	24pF	DLC70B
C9,C16	22pF	DLC70B
C15	12pF	DLC70B
C18,C20	10uF	10uF/50V
R1,R2	Chip Resistor,10ohm	1206
L1	12 turns, Inside diameter 3mm	
L2	7 turns, Inside diameter 3mm	
T2,T3	18 turns, Inside diameter 5mm	
T4,T5	7 turns, Inside diameter 3mm	

MV0530VX LDMOS TRANSISTOR

Document Number: MV0530VX
Preliminary Datasheet V3.0

Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate, 2—Drain, 3—Source)



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/6/22	Rev 1.0	Preliminary datasheet
2022/5/24	Rev 1.1	Modification of V4E package picture and drawing
2023/11/21	Rev 2.0	Modify drawing of extended leads length
2023/12/4	Rev 3.0	Finalized by changing to V4E1 package

Application data based on ZL-21-15

Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration. Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. "Typical" parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer's technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors

Copyright © by Innogration (Suzhou) Co.,Ltd.