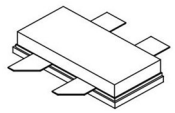
GaN HEMT 50V, 600W,2.1-2.2GHz RF Power Transistor

Description

STCV22603BY4



The STCV22603BY4 is a dual path 600watt , Input matched GaN HEMT, ideal for applications from 2.1 to 2.2GHz especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=300mA(Vgm=-3.07V，Vgp=-5.50V)

Pulsed CW: 20uS width, 10% cycle.

Freq (GHz)	Pulse CW Signal(1)				P_{avg}=50dBm WCDMA Signal(2)		
	P1 (dBm)	P1 (W)	P3 (dBm)	P3 (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
2.11	50.71	117	58.39	691	13.88	58.70	-31.20
2.14	49.26	85	58.28	672	13.86	59.00	-31.02
2.17	48.14	65	57.94	622	13.85	58.20	-30.30

Recommended driver: Class AB (1 stage discrete solution): STAV38041C6

Applications

- Asymmetrical Doherty amplifier within 2.1-2.2GHz
- S band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

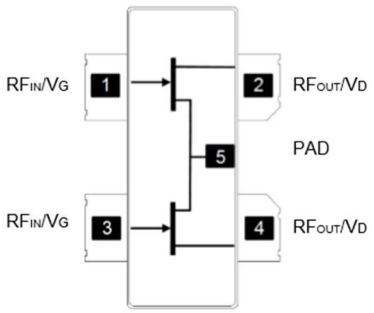


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc

Maximum gate current	Igs	83	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=90W, on Doherty application board	$R_{\theta JC}$	0.85	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=36mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 36mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.24		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=47mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 47mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.14GHz, Pout=90W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

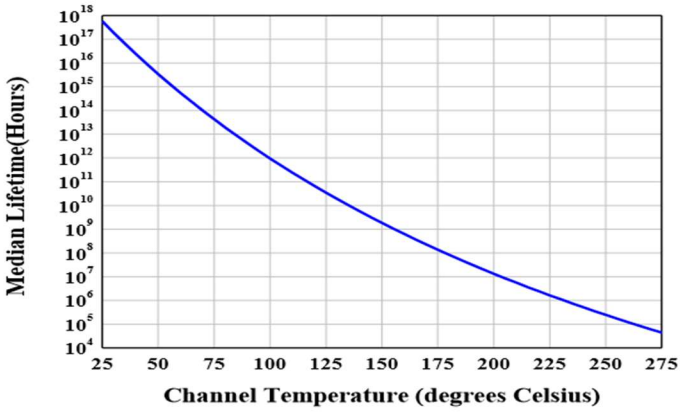
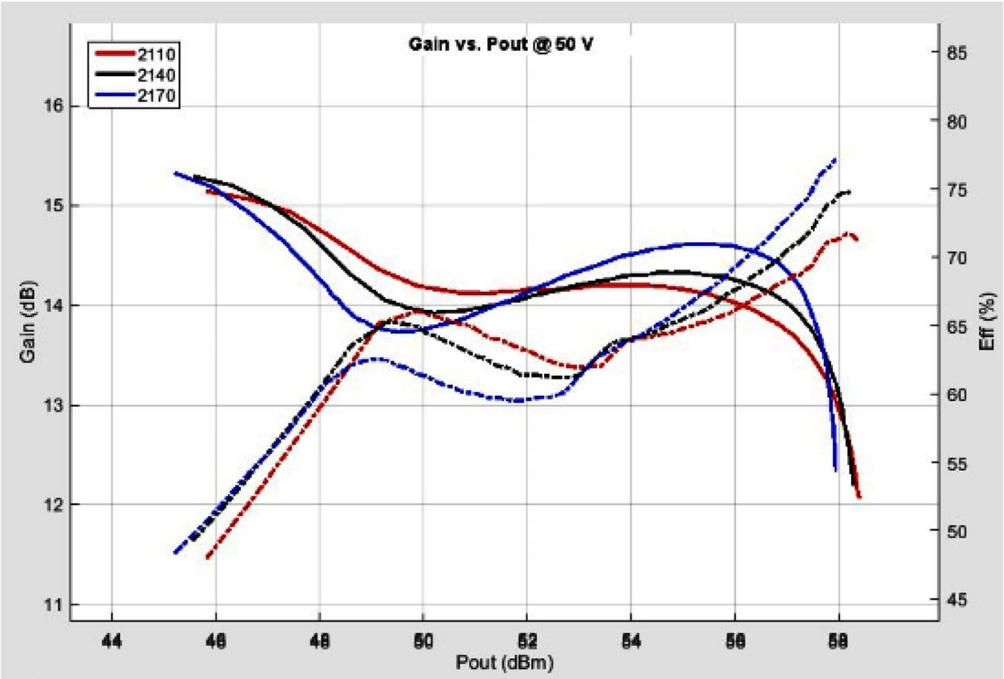


Figure 3: Efficiency and power gain as function of Pout (2.1-2.2GHz Doherty)



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2110	50.71	117.85	65.10	14.12	58.39	690.85	71.41
2140	49.26	84.27	65.16	14.05	58.28	672.33	74.92
2170	48.14	65.15	60.85	14.18	57.94	622.35	77.10

Figure 4: Network analyzer output, S11 and S21 (2.1-2.2GHz Doherty)

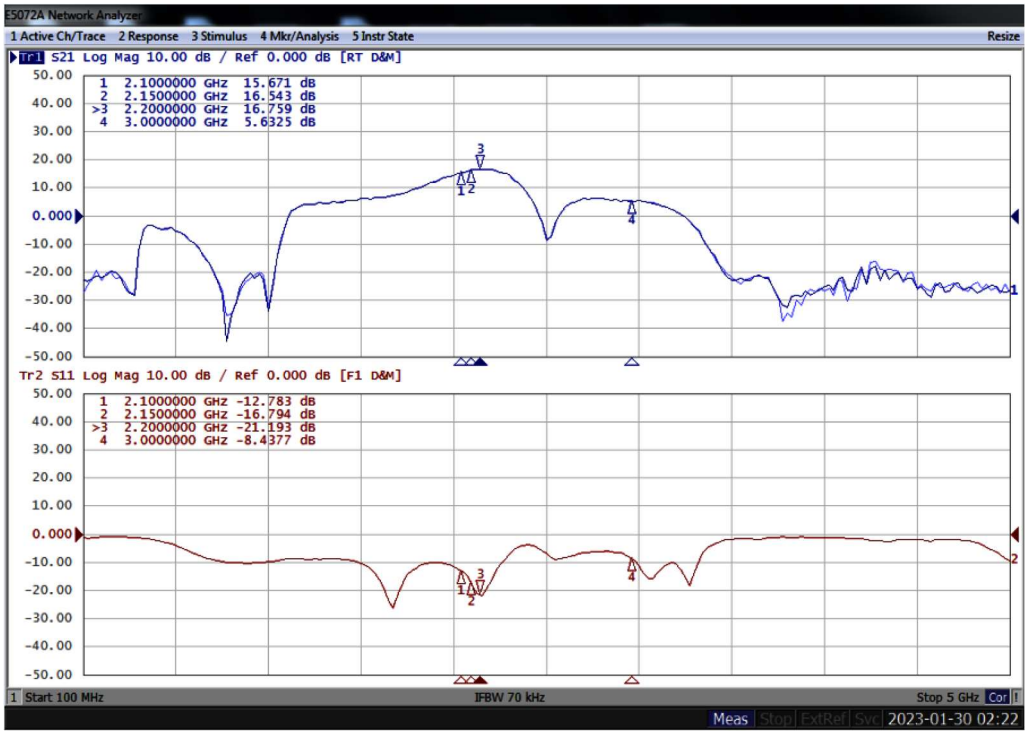


Figure 5: Picture of application board Doherty circuit for 2.1-2.2GHz

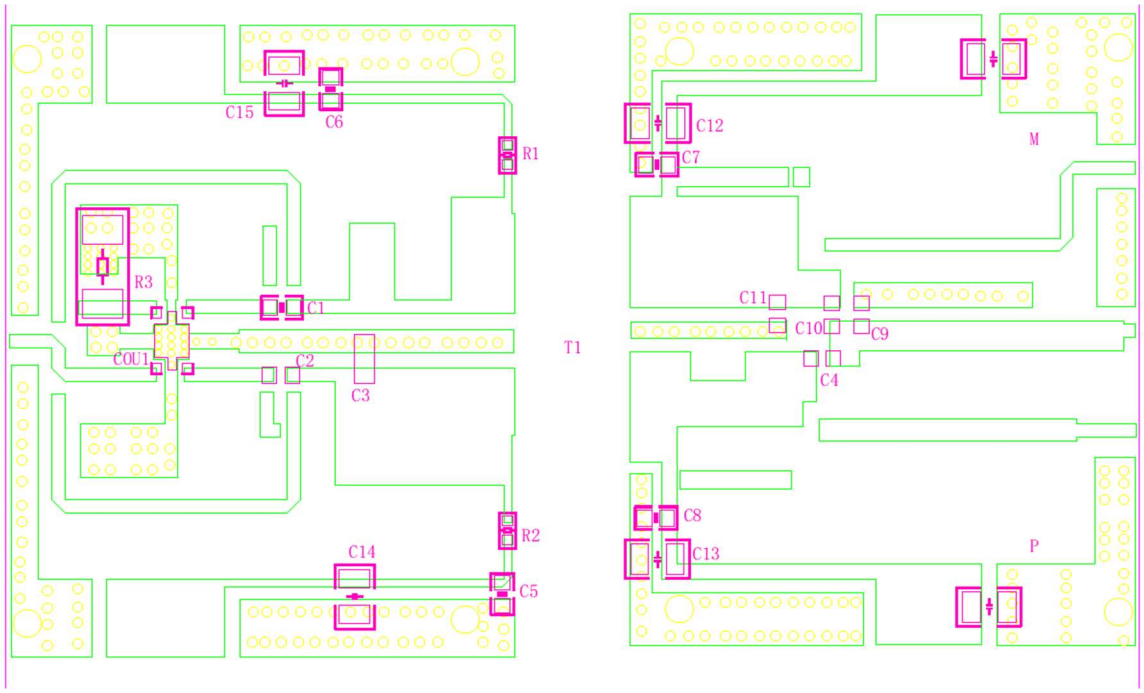
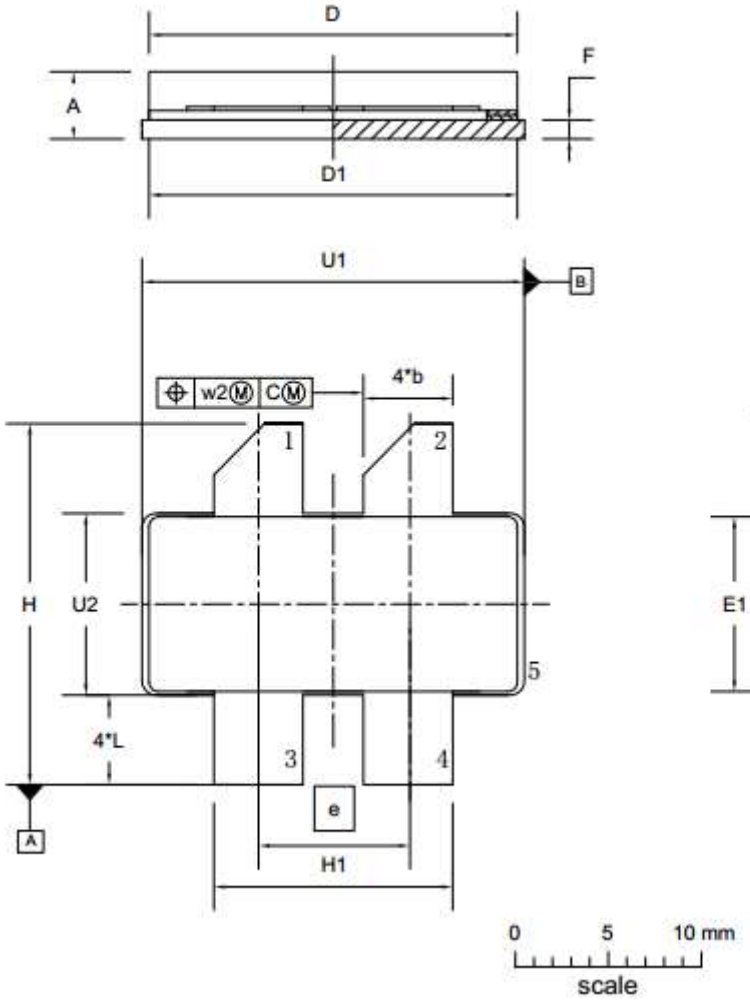


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Part	Quantity	Description	Part Number	Manufacture
C1,C2,C4,C5,C6,C7,C8	7	20pFHigh Q Capacitor	251SHS200BSE	TEMEX
C3,C11	2	1.1pFHigh Q Capacitor	251SHS1R1BSE	TEMEX
C9	1	0.2pFHigh Q Capacitor	251SHS0R2BSE	TEMEX
C12,C13,C14,C15	4	10uF MLCC	RS80R2A106M	MARUWA
C10	1	1.8pFHigh Q Capacitor	251SHS1R8BSE	TEMEX
R1,R2	2	10Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	51Ω Power Resistor	S1206N	RN2
COU1	1	3 dB Bridge	HC2100P03H	YANTEL
T1	1	600W GaN Dual Transistor	STCV22603BY4V	Innogration

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/1/30	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: LWH-23-02

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