## SME3010V GaN TRANSISTOR

## Gallium Nitride 50V 100W, RF Power Transistor

## Description

The SME3010V is a 100 -watt, unmatched GaN HEMT, designed for multiple applications with frequencies up to 3000 MHz . It can support CW, and pulsed CW, or any other modulated signal in form of saturated or back off conditions
There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

- Typical Pulsed CW RF performance (on fixture with device soldered):
SME3010V

VDS $=50 \mathrm{~V}$, $I D Q=70 \mathrm{~mA}$

| Freq <br> $(\mathrm{MHz})$ | P1dB <br> $(\mathrm{dBm})$ | P1dB <br> $(\mathrm{W})$ | P1dB <br> Eff $(\%)$ | P1dB <br> Gain $(\mathrm{dB})$ | P3dB <br> $(\mathrm{dBm})$ | P3dB <br> $(W)$ | P3dB <br> Eff $(\%)$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2400.00 | 49.86 | 96.77 | 68.85 | 17.06 | 51.00 | 125.92 | 74.08 |
| 2500.00 | 49.77 | 94.81 | 67.57 | 17.12 | 50.97 | 124.89 | 73.07 |
| 2600.00 | 49.62 | 91.67 | 65.90 | 16.97 | 50.93 | 123.77 | 71.92 |

CW data upon request

## Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC


## Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage ( 50 V )
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

## Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Drain--Source Voltage | $\mathrm{V}_{\mathrm{DSS}}$ | +200 | Vdc |
| Gate--Source Voltage | $\mathrm{V}_{G S}$ | -8 to 0 | Vdc |
| Operating Voltage | $\mathrm{V}_{\mathrm{DD}}$ | 0 to 55 | Vdc |
| Maximum forward gate current | lgf | 12 | mA |
| Storage Temperature Range | Tstg | -65 to +150 | C |
| Case Operating Temperature | $\mathrm{T}_{\mathrm{C}}$ | -55 to +150 | C |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +225 | C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, Junction to Case | ReJC | 2.6 | $\mathrm{C} / \mathrm{W}$ |
| $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, Pout=130W Pulsed CW, FEA |  |  |  |

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Table 3. Electrical Characteristics ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ unless otherwise noted)
DC Characteristics

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Drain-Source Breakdown Voltage | $\mathrm{V}_{G S}=-8 \mathrm{~V} ; \mathrm{I}_{\mathrm{DS}}=12 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{DSS}}$ |  | 200 |  | V |
| Gate Threshold Voltage | $\mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=12 \mathrm{~mA}$ | $\mathrm{~V}_{G S}(\mathrm{th})$ |  | -3.4 | V |  |
| Gate Quiescent Voltage | $\mathrm{V}_{\mathrm{DS}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DS}}=100 \mathrm{~mA}$, <br> Measured in Functional Test | $\mathrm{V}_{\mathrm{GS}(\mathrm{Q})}$ |  | -3.1 |  | V |

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system) : $\mathrm{V}_{\mathrm{DD}}=50 \mathrm{Vdc}, \mathrm{I}_{\mathrm{DQ}}=70 \mathrm{~mA}, \mathrm{f}=2500 \mathrm{MHz}$, Pulsed CW

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Gain | Gp |  | 14.5 |  | dB |
| Drain Efficiency@P3dB ${ }_{\text {t }}$ | Eff |  | 65 |  | \% |
| 3dB Compressed point | P3dB |  | 100 |  | W |
| Mismatch stress at all phases(No device damage) | VSWR |  | 10:1 |  | $\Psi$ |

Reference Circuit of Test Fixture Assembly Diagram


Figure 2. Test Circuit Component Layout ( $\mathbf{2 4 0 0} \mathbf{- 2 6 0 0 M H z}$ )
Table 4. Test Circuit Component Designations and Values

| Component | Value | Quantity |
| :---: | :---: | :---: |
| C1 C2 C3 C4 | 15 pF | 4 |
| C5 C6 | 10 uF | 2 |
| C7 | 470 uF | 1 |
| R1 | 10 ohm | 1 |
| C6 | 1.8 pF | 1 |

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Figure 3. Pulse RF performance


Figure 4. Network Analyzer result S11 and S21


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## Package Outline

Flanged ceramic package; 2 leads


Figure 1. Package Outline PKG-MME

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## Revision history

Table 5. Document revision history

| Date | Revision | Datasheet Status |
| :---: | :---: | :--- |
| $2023 / 1 / 30$ | V1.0 | Preliminary Datasheet Creation |
|  |  |  |
|  |  |  |

Application data based on ZXY-23-01

## Notice

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