



## DC-3.8GHz, 8W, 28V GaN Fully matched PA Module

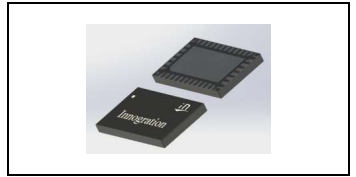
### Description

The GMAH0038-8 is a 8-watt ,single stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from 30MHz to 3.8GHz. The module is 50 Ω input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.

**When used at higher power supply up to 32V, it can be >10W across the 30MHz-3.8GHz. Or When extended to higher frequency up to 4GHz, it can be >6W at 28V and >8W at 32V across the full band from 30MHz-4GHz**

Vds=28V, Idq=30mA, CW



Parameter	30MHz	0.5GHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz	3.0GHz	3.8GHz	4.0GHz	Units
Small signal Gain	19.3	19.0	18.0	17.4	16.7	15.6	15.3	17.4	17.3	dB
Psat	9.5	8.5	9.6	9.6	10.2	9.3	9.5	7.9	6.2	W
Gain@Psat	16.3	16.0	15.0	14.4	13.7	12.6	12.3	14.4	14.3	dB
Eff@Psat	79	70	68	63	55	50	46	52	41	%

Vds=32V, Idq=30mA, CW

Parameter	30MHz	0.5GHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz	3.0GHz	3.8GHz	4.0GHz	Units
Small signal Gain	19.6	19.4	18.1	17.6	17.0	15.8	15.1	18.3	18.0	dB
Psat	11.5	10.8	12.5	12.6	12.1	10.6	11.0	10.2	8.1	W
Gain@Psat	16.6	16.4	15.1	14.6	14.0	12.8	12.1	15.3	15.0	dB
Eff@Psat	79	70	68	63	54	46	43	46	44	%

### Product Features

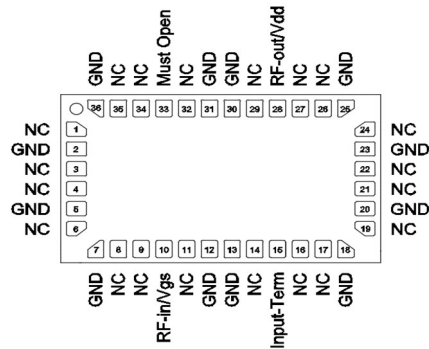
- Operating Frequency Range: DC-3.8GHz
- Operating Drain Voltage: +28 V (Up to 32V)
- 50 Ω Input/Output
- P3dB: ≥39dBm @28V, ≥10dBm @32V
- Small signal gain:>15dB, Power gain:>12dB
- Minimum efficiency:>40%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### Applications

- Ultra Broadband Amplifiers
- Fiber Drivers
- Test Instrumentation
- EMC Amplifier Drivers
- 2-way Radios



**Pin Configuration and Description**



Top View

Pin No.	Symbol	Description
28	RFout/Vdd	Transistor 1, Drain Bias & RF Output
10	RFin/Vgs	Transistor 1, RF Input & Gate Bias
15	Input-Term	Transistor 1, Input 50 ohm term
33	Must Open	Keep the pin open, no GND
1,3,4,6,8,9,11,14,16,17,19,21,22,24,26,27,29,32,34,35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	150	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +2	Vdc
Operating Voltage	$V_{DD}$	+36	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=87^\circ\text{C}$ , $T_j=175^\circ\text{C}$ , DC test	$R_{\theta JC}$	5	°C/W

**Table 3. Electrical Characteristics**

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		30		3800	MHz
Power Gain @ Psat		8			dB
$P_{SAT}$		39			dBm
Drain Efficiency @ $P_{SAT}$		40			%

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 28\text{ V}$ , Pulse Width=100 us, Duty cycle=10%

**Load Mismatch of per Section (On Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 30\text{ mA}$ ,  $f = 3.5\text{ GHz}$

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation
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## Reference Circuit of Test Fixture Assembly Diagram

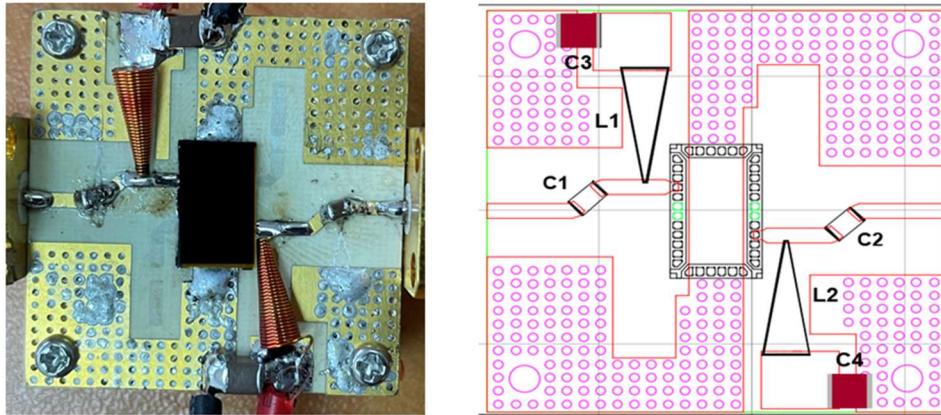


Figure 1. Test Circuit Component Layout

		Part NO. ↵	Vendor↵
C3, C4↵	10uF 100V chip Capacitor↵		↵
C1, C2↵	1uF Chip Capacitor↵	↵	ATC↵
L1, L2↵	0.45 uH 2.25A Inductor↵	CC31T30K240G5↵	Piconics↵
PCB↵	R04350B, 20mil, Er=3.48↵	↵	MTL↵

## TYPICAL CHARACTERISTICS

Figure 2. Network analyzer output S11/S21 (Pin=0dBm)

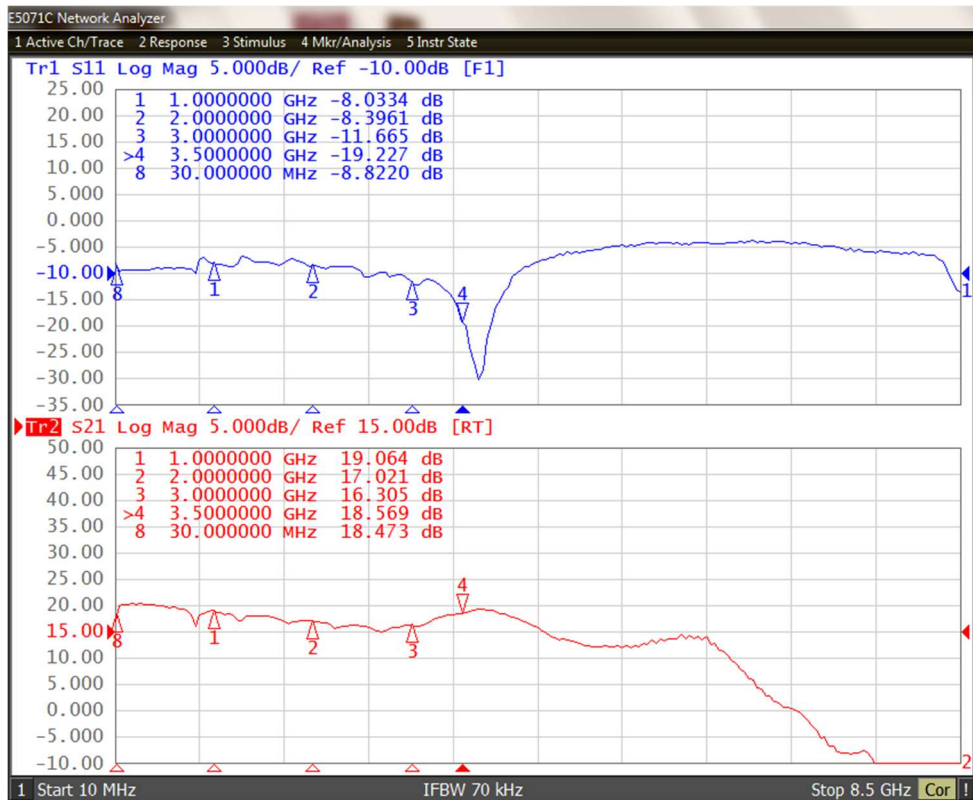
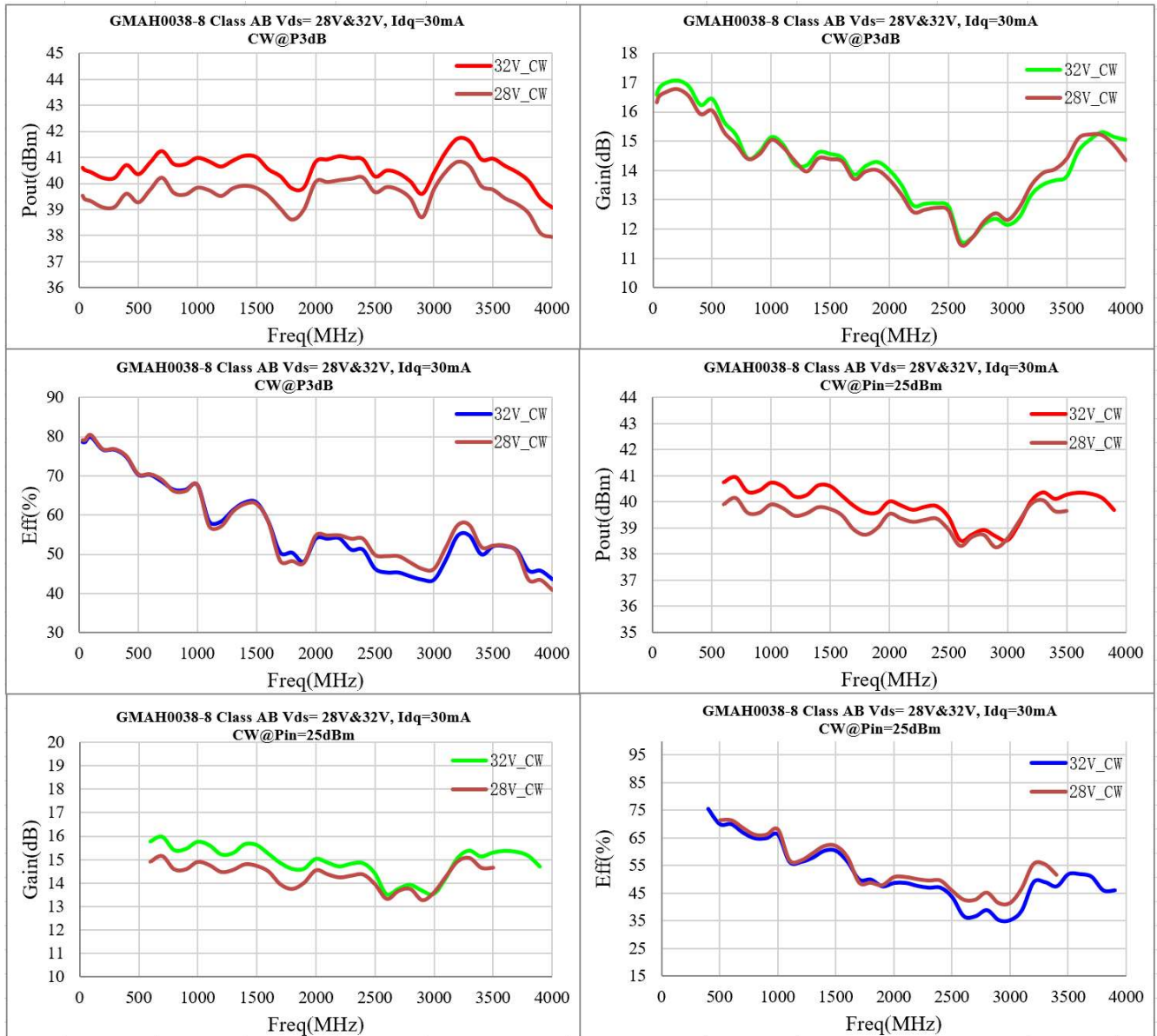


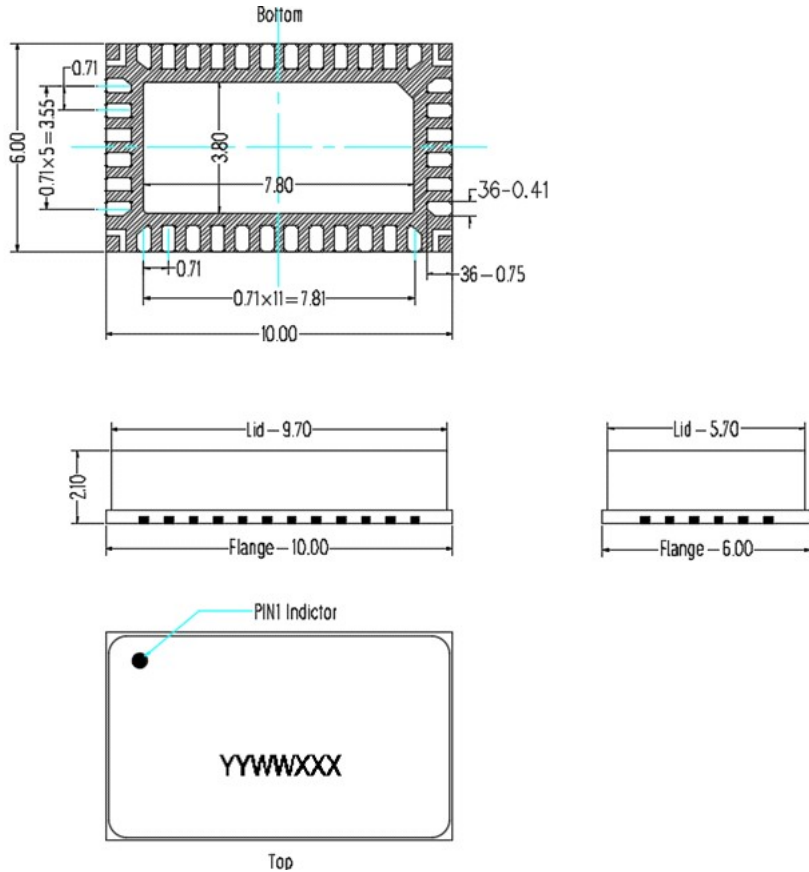


Figure 3. Psat, Power Gain and, efficiency and Pout @Pin=25dBm vs. Frequency



### Package Dimensions

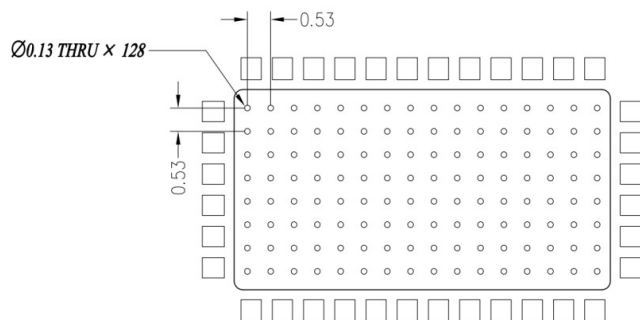
#### 10\*6 Plastic Package



**Notes:**

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2$ mm.

### Mounting Footprint Pattern



**Notes:**

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



## Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2022/12/9	Rev 1.0	Production Datasheet
2023/1/31	Rev 1.1	Modify the pin definition, highlight Pin 33 must be open

Application data based on ZHH-21-19

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