GaN HEMT 50V, 130W,1.8-2.2GHz Full band RF Power Transistor

STBV22W130C9

Description

The STBV22W130C9 is a dual path 130watt,Internally matched GaN HEMT, ideal for applications from 1.8 to 2.2GHz full band operation especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on **1.8-2.2GHz** full band asymmetrical Doherty with device soldered

VDS= 50V, IDQ=150mA(Vgm=-3.45V，Vgp=-5.4V)

ACPR @43dBm_1C-WCDMA			
Freq (MHz)	ACPR (dBc)	Gain (dB)	Efficiency (%)
1805	-28.93	14.38	56.46
1842.5	-29.20	14.69	58.38
1880	-29.51	14.91	59.06
2000	-28.57	14.99	57.20
2110	-28.27	14.73	57.38
2140	-28.15	14.71	57.16
2170	-28.02	14.92	56.04

(1)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Applications

- Asymmetrical Doherty amplifier within 1.8-2.2GHz full band
- Sub-2GHz power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

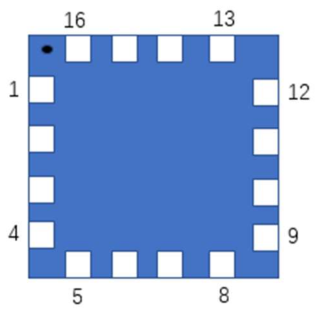
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
1,2	RF IN/Vgs of Main	RF Input/Gate bias of main path
3,4	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
9,10	RF OUT/Vds of Peak	RF Output/Drain bias of peak path

11,12	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back off applications, but will result in higher junction temperatures

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	27	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=20W, on Doherty application board	RθJC	3.5	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=6mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 6mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=10mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 10mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=200mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.14GHz, Pout=20W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

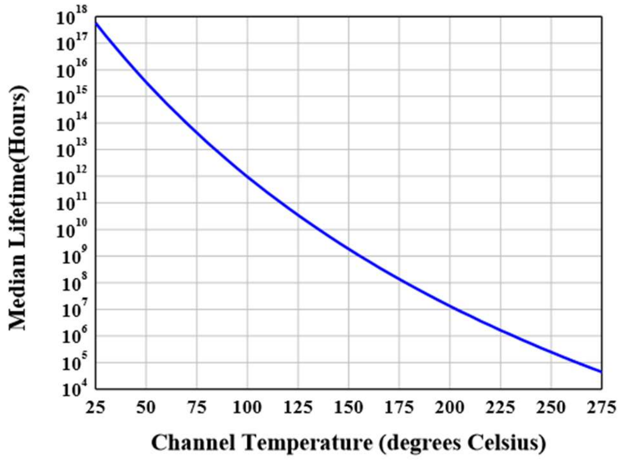
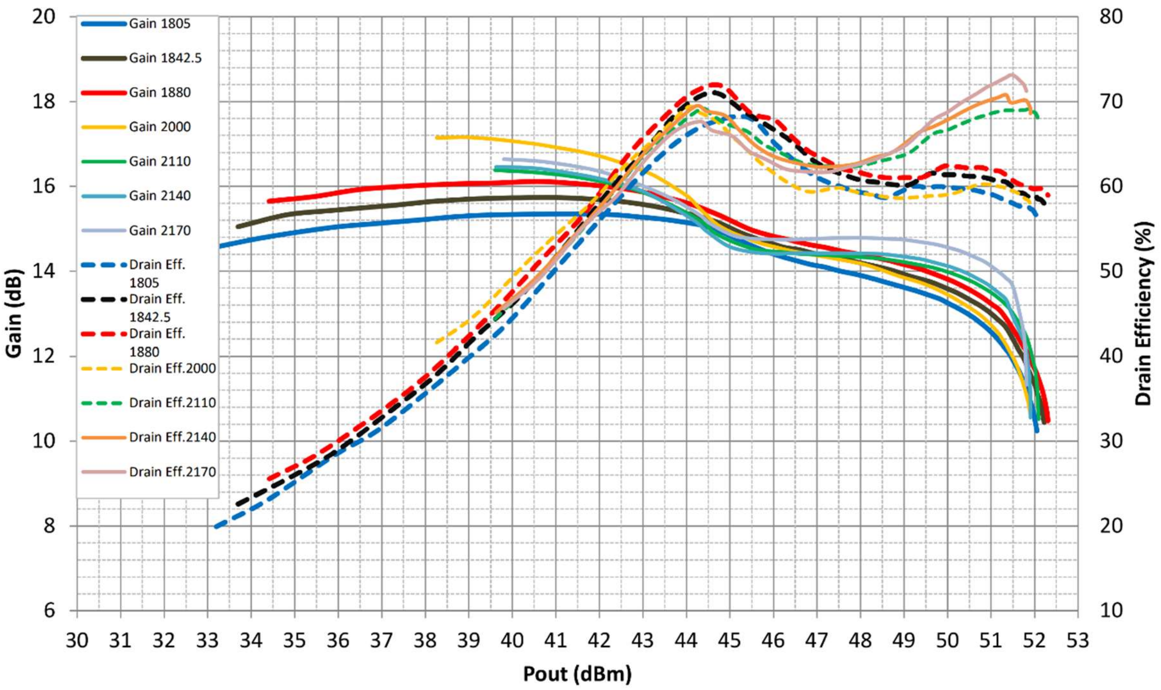


Figure 3: Efficiency and power gain as function of Pout (1.8-2.2GHz Doherty)



Freq	P3dB	P3dB	P3dB Eff	P1dB Gain	P5dB	P5dB	P5dB Eff
(MHz)	(dBm)	(W)	%	dB	(dBm)	(W)	%
1805	51.24	133.18	58.55	14.18	52.06	160.55	56.53
1842.5	51.35	136.60	60.48	14.58	52.22	166.63	57.98
1880	51.23	132.78	61.71	14.98	52.31	170.04	58.96
2000	48.18	65.73	59.07	15.76	51.89	154.66	57.99
2110	51.29	134.52	68.93	15.18	52.09	161.96	67.60
2140	51.34	136.27	70.78	15.17	51.90	155.05	68.59
2170	51.50	141.36	73.12	15.32	51.81	151.77	71.23

Figure 4: Network analyzer output, S11 and S21 (1.8-2.2GHz Doherty)

m4 freq=385.9 MHz dB(S(2,1))=11.124 dB(S(1,1))=-1.999	m8 freq=2.110 GHz dB(S(2,1))=18.139 dB(S(1,1))=-25.568	m6 freq=2.140 GHz dB(S(2,1))=18.135 dB(S(1,1))=-30.617	m7 freq=2.170 GHz dB(S(2,1))=18.104 dB(S(1,1))=-29.977
m1 freq=1.805 GHz dB(S(2,1))=17.130 dB(S(1,1))=-34.114	m2 freq=1.843 GHz dB(S(2,1))=17.525 dB(S(1,1))=-34.377	m3 freq=1.880 GHz dB(S(2,1))=17.831 dB(S(1,1))=-32.620	m5 freq=2.000 GHz dB(S(2,1))=18.140 dB(S(1,1))=-22.972

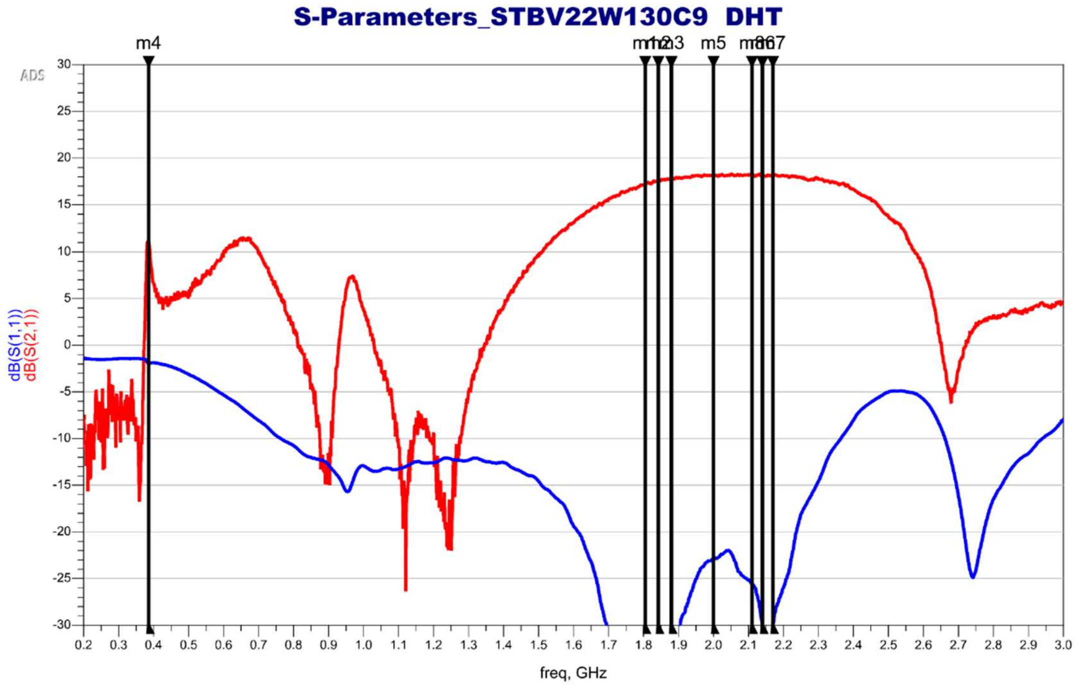


Figure 5: Picture of application board Doherty circuit for 1.8-2.2GHz

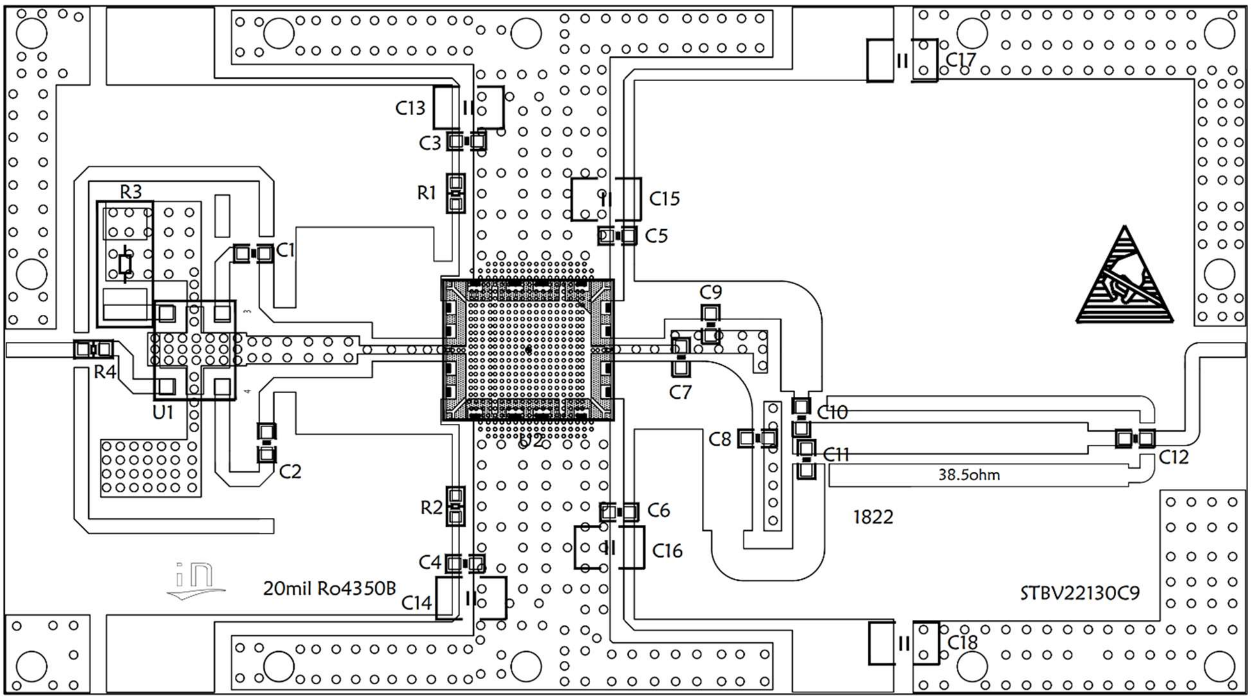
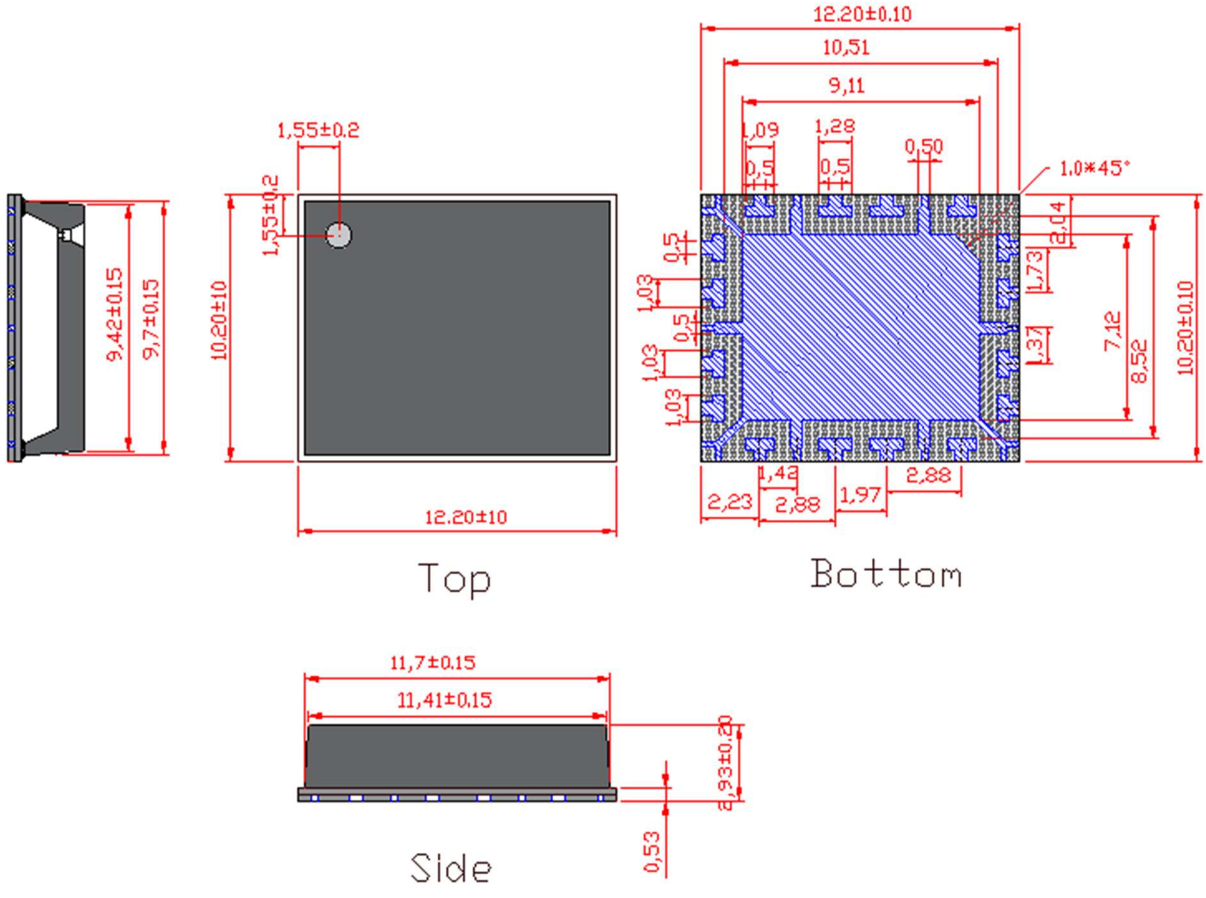


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6, C11, C12	0603	20pF/250V	8
C7	0603	2.7pF/250V	1
C8	0603	1.6pF/250V	1
C9	0603	0.6pF/250V	1
C10	0603	4.3pF/250V	1
C13, C14	0805	10uF/16V	2
C15, C16, C17, C18	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	2512	50R	1
R4	0603	0R	1
U1	6.35x5.08mm	HC2100P03H	1
U2	C9	STBV22W130C9[V3]	1

Package Dimensions （Unit:mm）



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/1/16	V1.0	Preliminary Datasheet Creation
2023/1/31	V1.1	Update the package drawing to be more understandable for soldering
2023/8/17	V1.2	Modification of package drawing on last page
2023/11/16	V1.3	Update based on application report of rev 3

Application data based on: ZBB-23-03/33

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