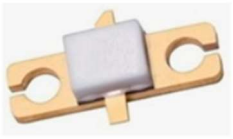
SME6006V GaN TRANSISTOR

Document Number: SME6006V
Product Datasheet V1.0

Gallium Nitride 50V 60W, RF Power Transistor

SME6006V



Description

The SME6006V is a 60W single ended, unmatched GaN HEMT, designed for multiple applications with frequencies up to 4.2GHz.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical performance (on Innogration narrow band production fixture with device soldered)

V_{DD}=50V I_{DQ}=15mA, Pulse CW, pulse width: 20us, duty cycle: 10%

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
3400	47.72	59.2	62.2	14.28	48.63	73.0	63.0
3500	47.51	56.3	62.3	14.81	48.46	70.1	63.3
3600	46.39	43.5	59.2	14.77	47.72	60.2	62.8

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	8	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC Power Dissipation, FEA	$R_{\theta JC}$	4.1	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=8mA	V_{DSS}		200		V
Gate Threshold Voltage	V_{DS} = 50V, I_D = 8mA	V_{GS}(th)		-3.4		V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system) : V_{DD} = 50 Vdc, I_{DQ} = 15 mA, f = 3500 MHz, Pulse CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P3dB	Gp		12		dB
Drain Efficiency@P3dB$_t$	Eff	60			%
3dB Compressed point	P3dB	60			W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		Ψ

Reference Circuit of Test Fixture Assembly Diagram

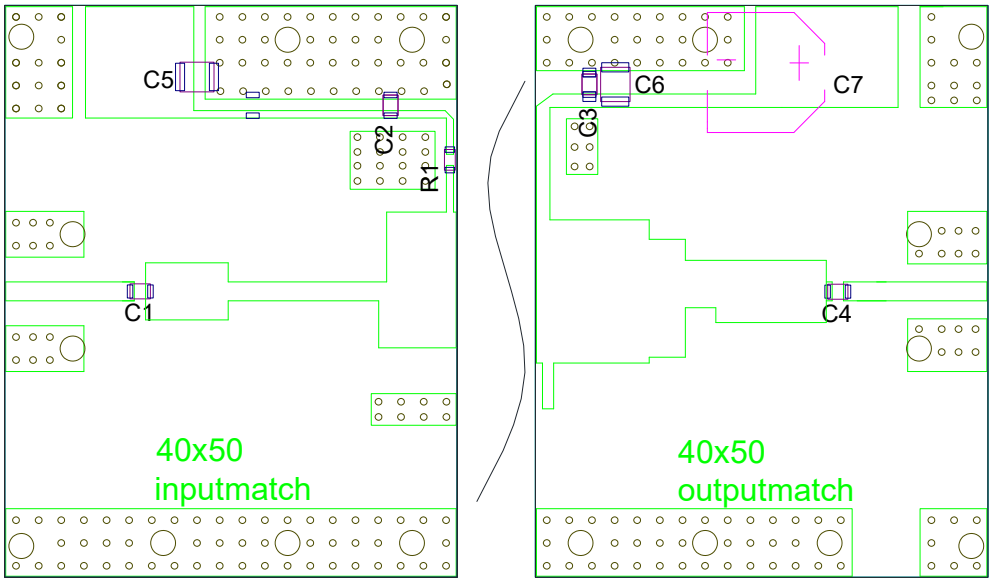


Figure 1. Test Circuit Component Layout (3400-3600MHz)

Table 4. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C3, C4	0805	6.8 pF	4
C5, C6	1210	10uF/100V	2
C7		100uF/63V	1
R1	0603	10R	1

Figure 2. Power Gain and Efficiency Vs frequency

Vgs = -3.09V, VDS= 50V, IDQ = 100mA, Pulsed CW, 20uS width, 10% dule cycle.

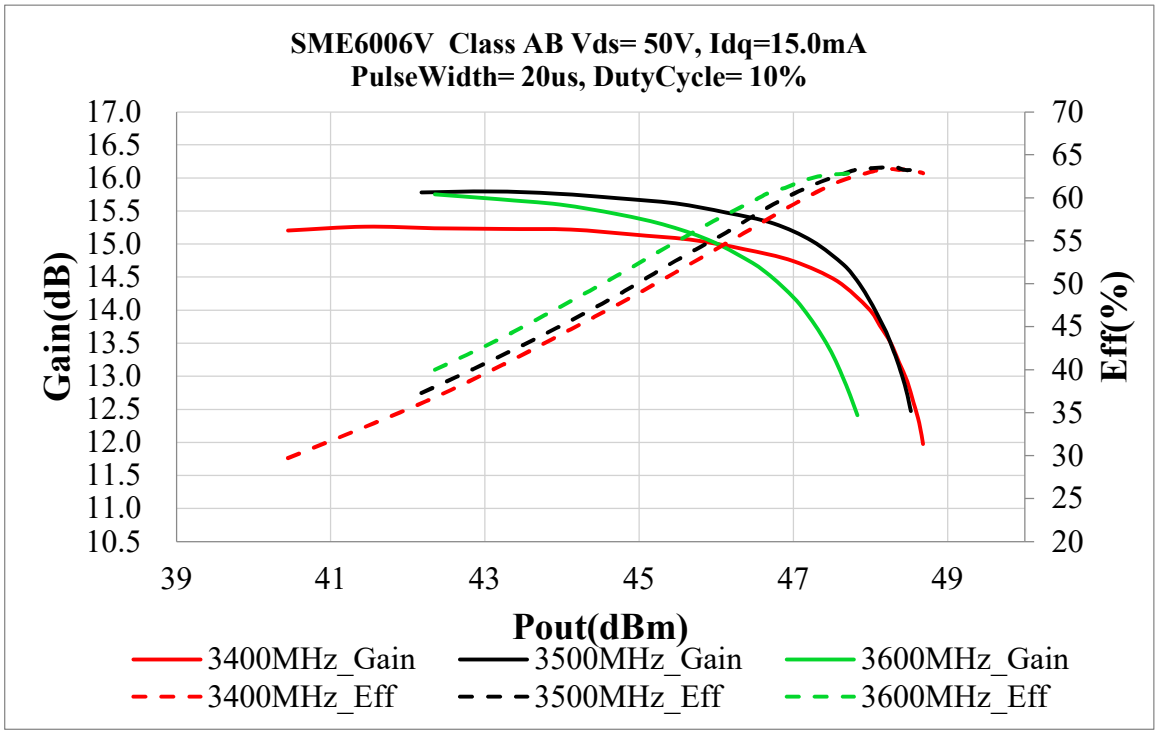
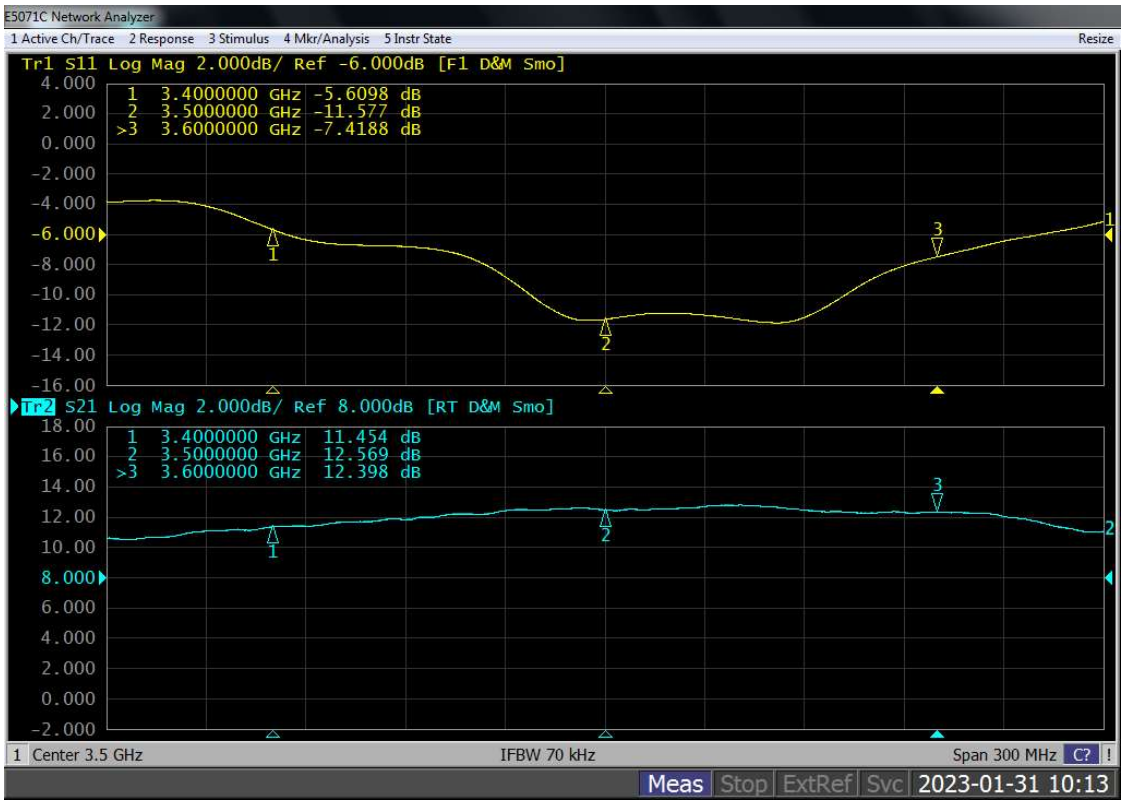
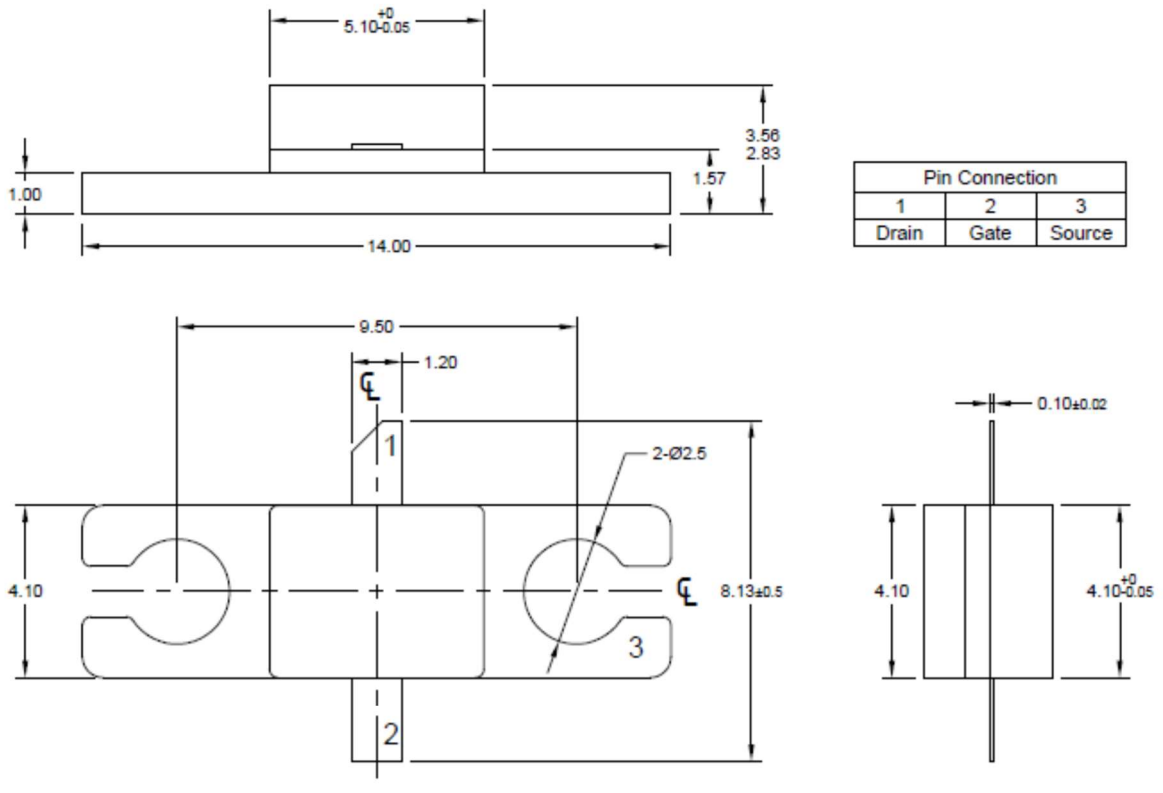


Figure 3. Network Analyzer result S11 and S21 Vgs = -3.09V, VDS= 50V, IDQ = 100mA



Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MME					10/10/2016

Figure 1. Package Outline PKG-MME

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/1/31	V1.0	Product Datasheet

Application data based on LSM-23-03

Notice

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