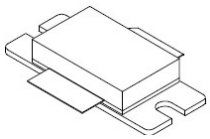
MZ1245V LDMOS TRANSISTOR

Document Number: MZ1245V
Product Datasheet V1.0

450W, 50V High Power RF LDMOS FETs

MZ1245V



Description

The MZ1245V is a 450-watt, high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 960 to 1215MHz.

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical Performance (on innogration wide band test fixture with device soldered):
  Pulse width:100uS, duty cycle: 10%, TA = 25 °C Vds = 50 V, Idq = 200 mA

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	IDS （A）	Gain (dB)	Eff (%)
960	41.60	57.50	562.3	2.29	15.90	54.3
980	42.00	57.40	549.5	2.30	15.40	53.1
1000	42.20	57.30	537.0	2.30	15.10	51.9
1020	41.90	57.50	562.3	2.35	15.60	53.1
1040	41.90	57.50	562.3	2.32	15.60	53.8
1060	42.20	57.47	558.5	2.34	15.27	53.2
1080	42.00	57.20	524.8	2.27	15.20	51.6
1100	42.00	57.34	542.0	2.33	15.34	51.8
1120	42.10	57.36	544.5	2.33	15.26	52.1
1140	42.20	57.23	528.4	2.29	15.03	51.6
1160	42.30	57.30	537.0	2.24	15.00	53.7
1180	42.22	57.28	534.6	2.28	15.06	52.4
1200	42.20	57.28	534.6	2.24	15.08	53.5
1215	41.90	57.01	502.3	2.12	15.11	53.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	VDSS	115	Vdc
Gate--Source Voltage	VGS	-10 to +10	Vdc
Operating Voltage	VDD	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 500W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, I_{DQ} = 200 mA, frequeny:1090MHz	$R_{\theta JC}$	0.03	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.3		V

Functional Tests (In Innogration test fixture, 50 ohm system) :V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 1215MHz, Pulse CW Signal Measurements.

(Pulse Width=100 μs, Duty cycle=10%), Pin=42dBm

Power Gain @ Pout	G_p		15		dB
Output Power	Pout	450	500		W
Drain Efficiency@Pout	η_D		50		%

Reference Circuit of Test Fixture Assembly Diagram

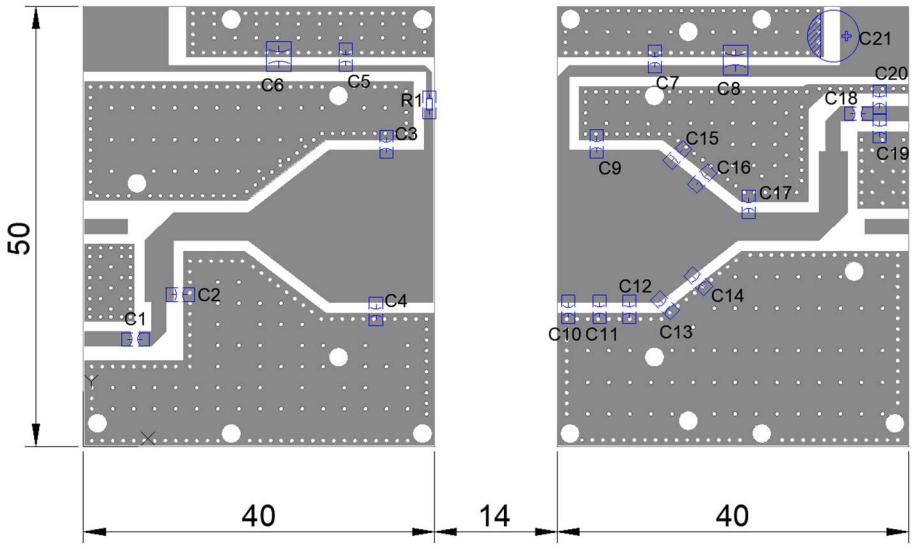
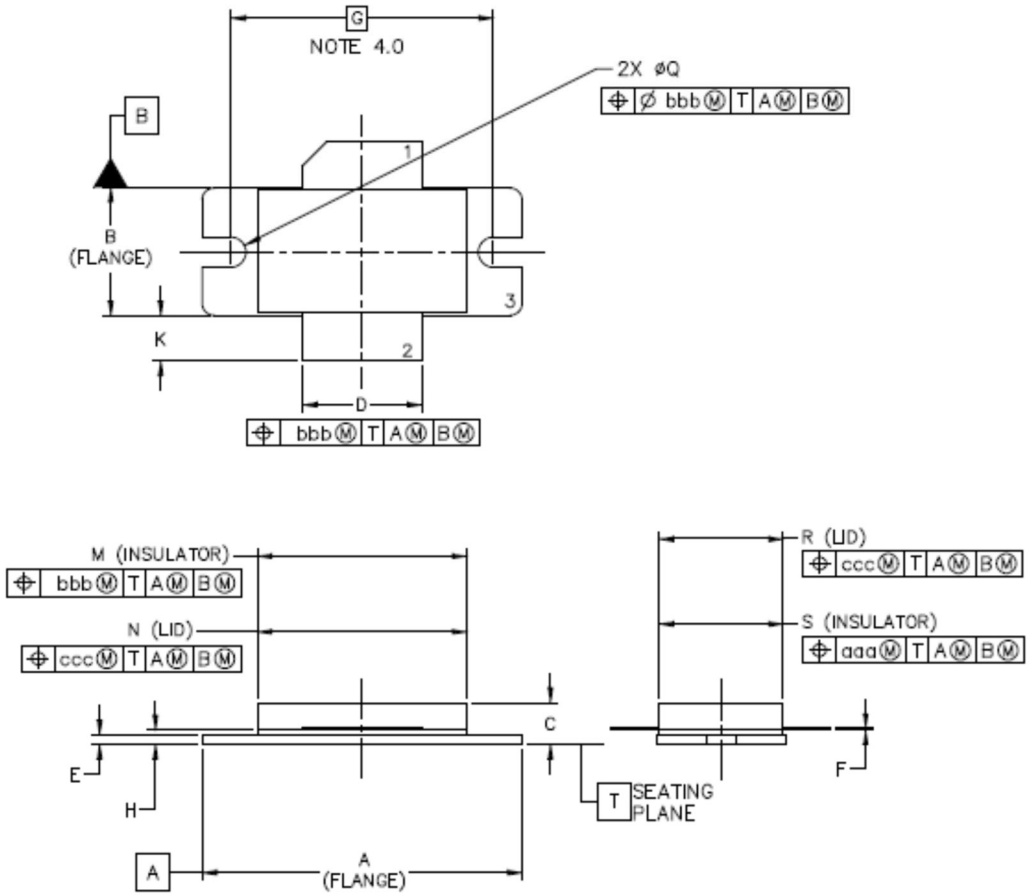


Table 5. Test Circuit Component Designations and Values

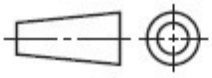
Component	Description	Suggested Manufacturer
C1,C5, C7, C18,	33pF	ATC800B
C3,C4,	4.7pF	ATC600F
C2, C12,	1.8pF	ATC800B
C9,	5.1pF	ATC800B
C10,	6.8pF	ATC800B
C11,C19	0.8pF	ATC600F
C13, C15,C17,C20	1.2pF	ATC600F
C14, C16,	2pF	ATC800B
C6,C8	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C21	470uF	50V/2200uF
R1	Chip Resistor,10 Ω	1206
PCB	30Mil Rogers4350B	

Package Outline

PACKAGE DIMENSIONS



DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.515	.525	13.08	13.34
B	.535	.545	13.59	13.84	S	.515	.525	13.08	13.34
C	.147	.200	3.73	5.08	aaa	–	.007	–	0.178
D	.495	.505	12.57	12.83	bbb	–	.010	–	0.254
E	.035	.045	0.89	1.14	ccc	–	.015	–	0.381
F	.003	.006	0.08	0.15	–	–	–	–	–
G	1.100 BSC		27.94 BSC		–	–	–	–	–
H	.057	.067	1.45	1.70	–	–	–	–	–
K	.175	.205	4.45	5.21	–	–	–	–	–
M	.872	.888	22.15	22.56	–	–	–	–	–
N	.871	.889	22.12	22.58	–	–	–	–	–
Q	ø.118	ø.138	ø3.00	ø3.51	–	–	–	–	–

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-Z2E					09/19/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/1/4	Rev 1.0	Product Datasheet Creation

Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration . Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose.“Typical” parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer’s technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors