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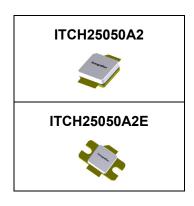
2300MHz-2500MHz, 50W, 28V RF Power LDMOS FETs

Description

The ITCH25050A2 is a 50-watt , internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 2300MHz to 2500 MHz $_{\circ}$

• Typical Performance of 2400-2500MHz (On Innogration fixture with device soldered): $V_{DD} = 28 \text{ Volts, } I_{DQ} = 100 \text{ mA} \text{ , Pulse Width = 10us, Duty Cycle = 12\%}.$

Freq(MHz)	P1(dBm)	Gain@P1(dB)	P3(dBm)	Eff(%)@P3
2400	48.1	16.7	48.8	59.6
2450	47.9	17.1	48.6	61.3
2500	47.4	17.3	48.1	60.8



 $\bullet \mbox{Typical Performance of 2400-2500MHz (On Innogration fixture with device soldered):} \\$

 V_{DD} = 32 Volts, I_{DQ} = 100 mA , CW.

Freq(MHz)	P1(dBm)	Gain@P1(dB)	P3(dBm)	Eff(%)@P3
2400	48.7	16.8	49.3	57.2
2450	48.5	17.1	49.1	58.3
2500	48.2	17.5	48.8	59.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- · Excellent thermal stability, low HCI drift

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+69	Vdc
GateSource Voltage	V_{GS}	-7 to +10	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T₃	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Rеjc	0.9	°C/W
T_C = 85°C, T_J =200°C, DC test			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit



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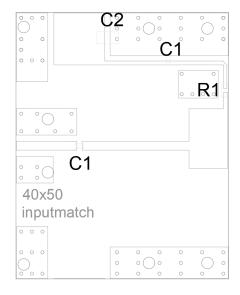
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Drain-Source Breakdown Voltage	n-Source Breakdown Voltage V _{GS} =0V; I _{DS} =1mA		65			V
Zero Gate Voltage Drain Leakage Current	V _{DS} = 28 V, V _{GS} = 0 V	I _{DSS}			1	μА
GateSource Leakage Current	V _{GS} = 9 V, V _{DS} = 0 V	I _{GSS}			1	μА
Gate Threshold Voltage	V_{DS} = 28V, I_{D} = 300 μA	V _{GS} (th)	1.5	2.0	2.5	V
Gate Quiescent Voltage	V_{DS} = 28 V, I_{DS} = 100 mA, Measured in Functional Test	V _{GS(Q)}	2.2	2.7	3.2	V

CW performance (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 32 \text{ Vdc}$, $I_{DQ} = 100 \text{ mA}$, f = 2400-2500 MHz, CW.

Characteristic	Symbol	Min	Тур	Max	Unit
Power Gain @ P1dB	Gp	15.5	17		dB
Drain Efficiency @ P3dB	η _D	52	58		%
3dB Compression Point	P _{-3dB}	48	49.5		dBm
Input Return Loss	IRL		-7		dB

Reference Circuit



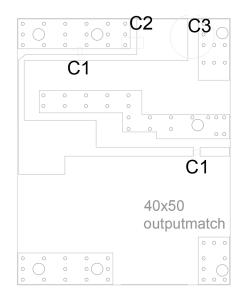


Figure 1. Test Circuit Component Layout (2400MHz~2500MHz)

Table 5. Test Circuit Component Designations and Values

Component	Description
C1	15pF, high Q capacitance
C2	10uF/63V
R1	10 Ω
С3	470uF/63V
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper



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TYPICAL CHARACTERISTICS

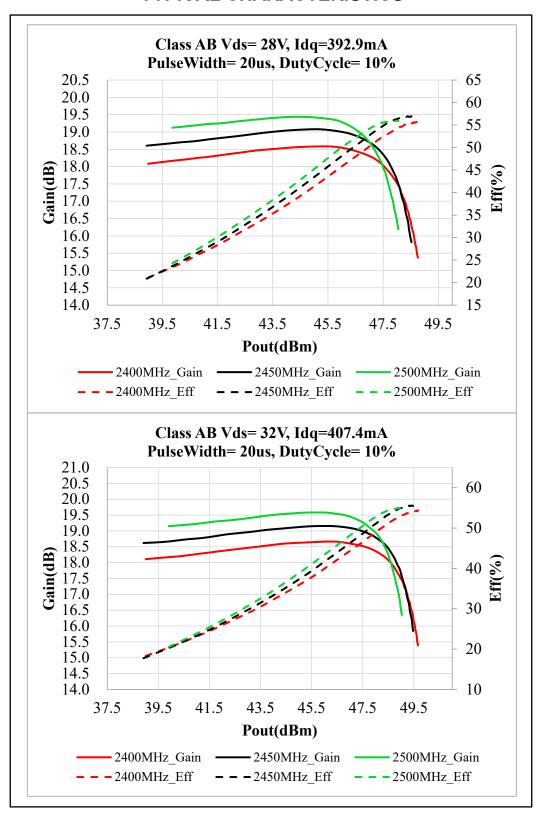
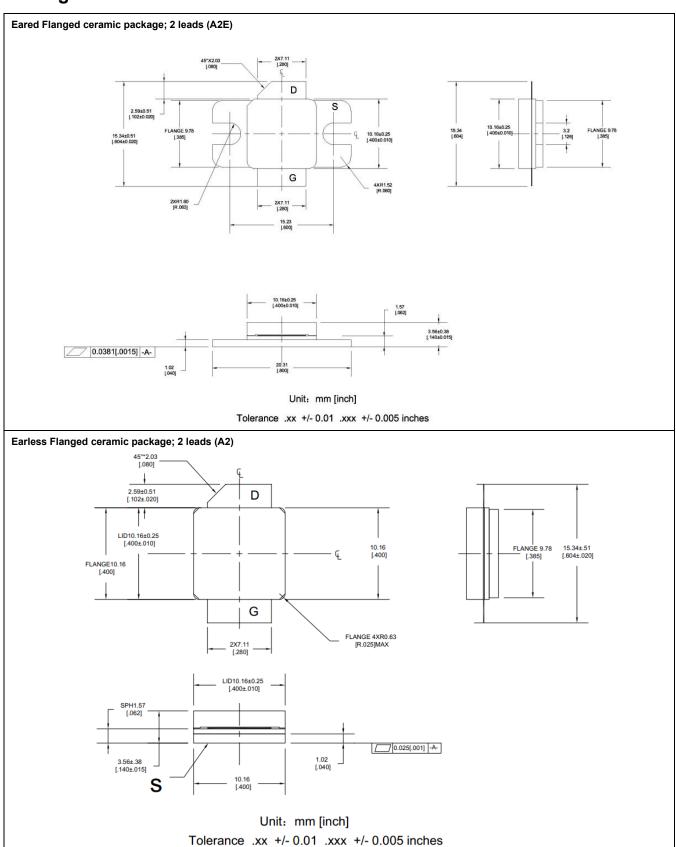


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power

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Package Outline





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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2021/6/16	Rev 1.0	Preliminary Datasheet
2023/2/23	Rev 2.0	Update test data
2023/12/21	Rev 2.1	Update parameters

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