



GaN 50V, 500W, 2.3-2.5GHz RF Power Transistor

Description

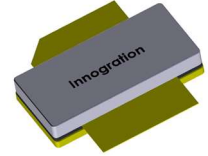
The S3K2550VS is a single ended 500watt capable, GaN HEMT, ideal for any applications within 2.3-2.5GHz

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical Pulsed CW performance at **2.3-2.5GHz** applications

$V_{DD} = 50$ Vdc, $V_{GS} = -3.35$ V, $I_{DQ} = 100$ mA , with device soldered, 400us, 20%

S3K2550VS



Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout (W)	IDs(A)	Gain(dB)	效率 (%)
2300	43.11	57.84	608.14	4.02	14.73	60.48
2320	43.52	57.87	612.35	4.06	14.35	60.33
2340	43.34	57.83	606.74	4.0	14.49	60.67
2360	42.74	57.77	598.41	3.93	15.03	60.91
2380	42.25	57.67	584.79	3.81	15.42	61.40
2400	42.7	57.7	588.84	3.69	15.0	63.83
2420	42.6	57.63	579.43	3.69	15.03	62.81
2440	43	57.56	570.16	3.59	14.56	63.53
2460	42.84	57.45	555.90	3.49	14.61	63.71
2480	42.52	57.23	528.45	3.31	14.71	63.86
2500	43.26	57.09	511.68	3.21	13.83	63.76

Applications

- Microwave communication
- 2.45GHz ISM application
- S band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{GS}	68	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C



Operating Junction Temperature	T_J	+225	$^{\circ}\text{C}$
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Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C=25^{\circ}\text{C}$, at $P_{out}=550\text{W}$ Pulsed at 2.4GHz	$R_{\theta JC}$	0.7	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}$; $I_{DS}=68\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS}=10\text{V}$, $I_D=68\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS}=50\text{V}$, $I_{DS}=120\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Ruggedness Characteristics

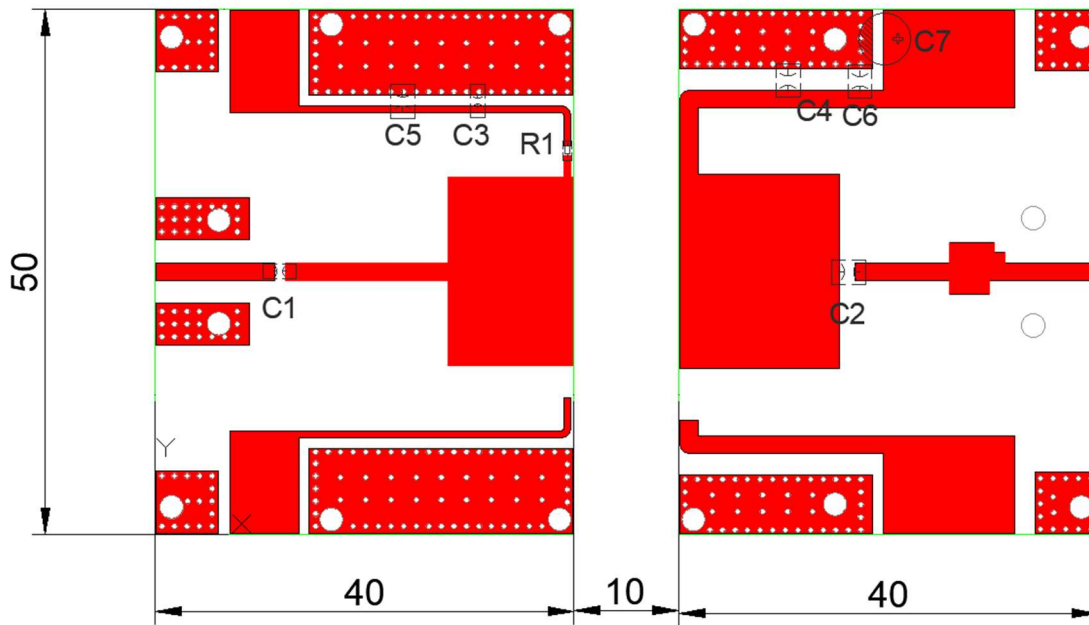
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.4GHz, $P_{out}=550\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

TYPICAL CHARACTERISTICS

Figure 2: S11/S21 output from Network analyser ($V_{DS}=50\text{V}$, $I_{DQ}=500\text{mA}$ $V_{gs}=-3.26\text{V}$)



Figure 3: Reference design circuit (PCB DWG file upon request,)

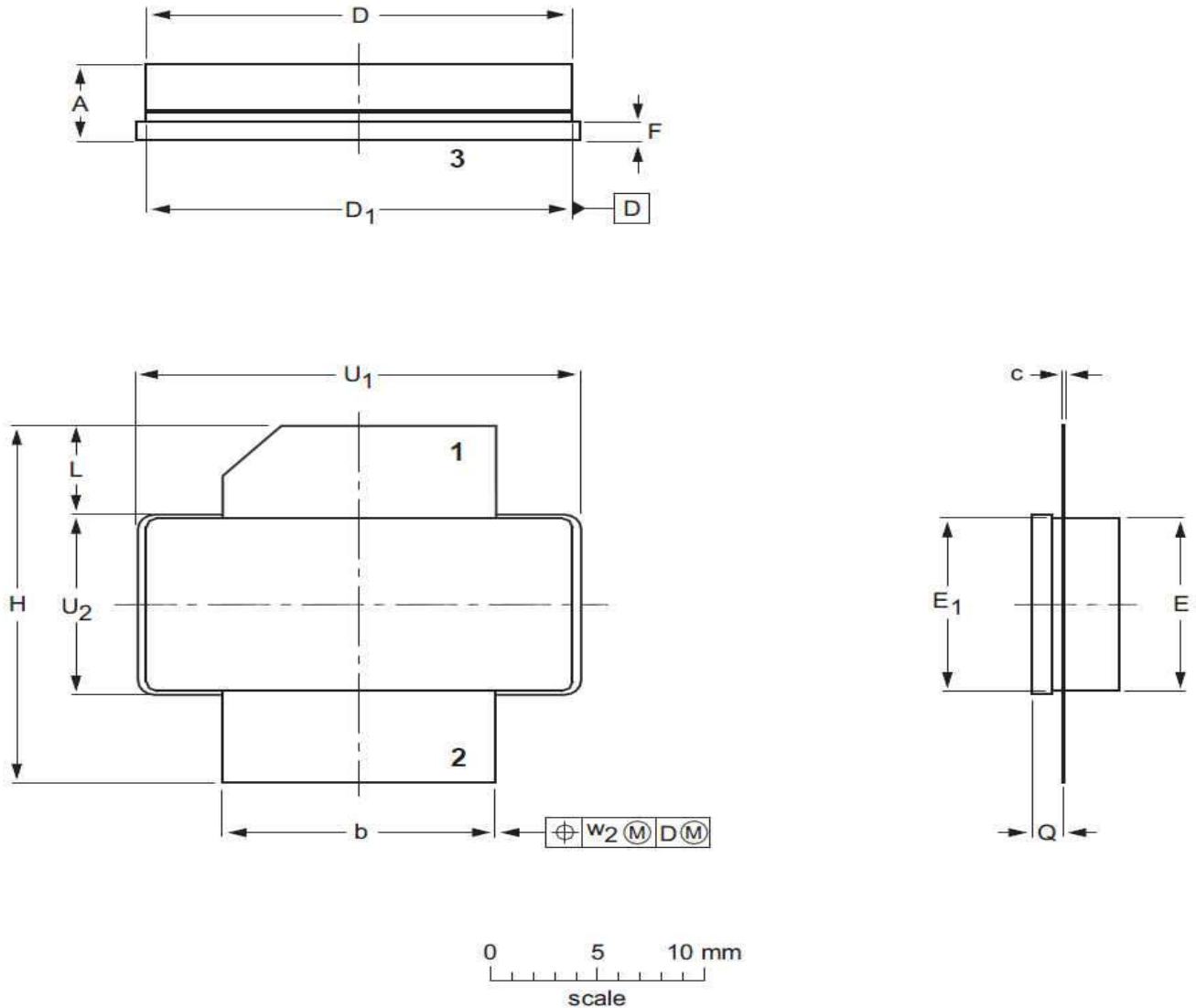


Component	Description	Suggested Manufacturer
C1,C2	15pF	ATC800B
C3,C4	18pF	ATC800B
C5,C6,	Ceramic multilayer capacitor, 10uF, 100V	1210
C7	4700uF/63V	
R1	Chip Resistor, 10 Ω	0805
PCB	board material: Rogers 4350B, $\epsilon_r = 3.5$, thickness 30 mils, 1oz copper on each side	



Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/2/6	V1.0	Preliminary Datasheet Creation

Application data based on: YHG-23-03

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