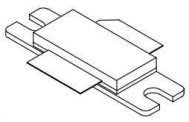
MK1510V LDMOS TRANSISTOR

Document Number: MK1510V
Preliminary Datasheet V2.0

150W, 0.7-1.5GHz 50V High Power RF LDMOS

MK1510V



Description

The MK1510V is a 150W P1dB single ended 50V LDMOS, internally matched for any applications within 0.7-1.5GHz

It is suitable for use in avionics application of 960-1215MHz, and L band application of 1200-1400MHz.

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

- Typical performance(on 960-1215MHz application board with devices soldered)

V_{DS}=50V,Idq=20mA, Pulsed CW, 10% duty cycle, 10us pulse width

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	52.57	180.7	62.9	15.19	53.01	200.1	63.3
1030	51.96	156.9	53.6	15.89	52.5	177.7	53.8
1090	52.04	159.9	48.5	14.93	52.62	182.7	49.3
1150	52.58	181.2	51.6	14.48	53.07	202.8	52.0
1215	52.41	174.3	58.9	15.46	52.79	190.1	58.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 C, 150 W Peak, 10usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1030 MHz	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 20 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.18		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 20mA, f = 1030MHz, pulse width:10us, duty cycle:10%, Pout=150W

VSWR: > 7:1 at All Phase Angles	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout within 960-1215MHz at different drain voltage

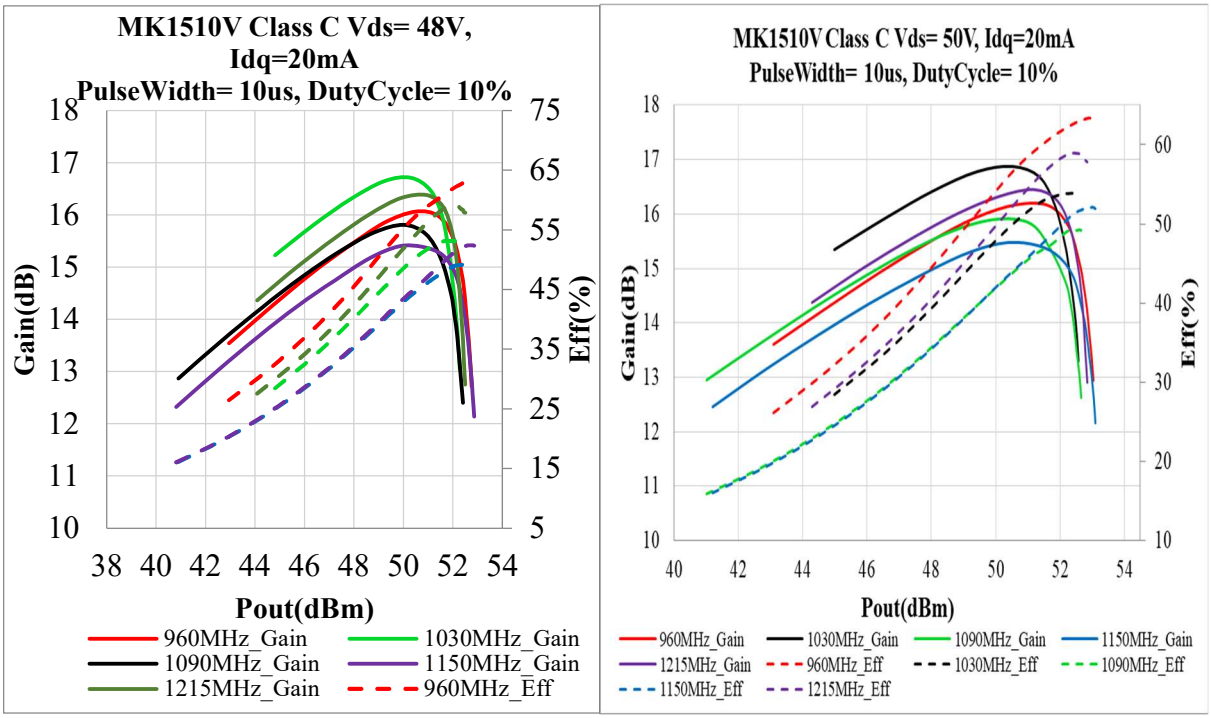


Figure 2: Network analyzer output S11/S21 at 50V Idq=450mA

Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

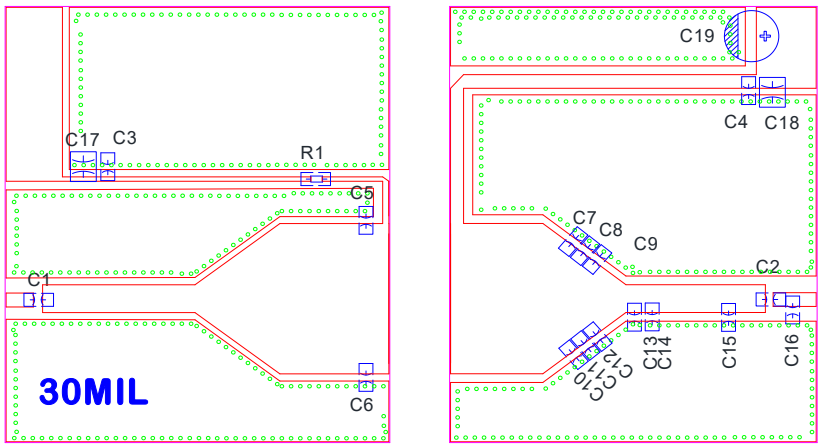
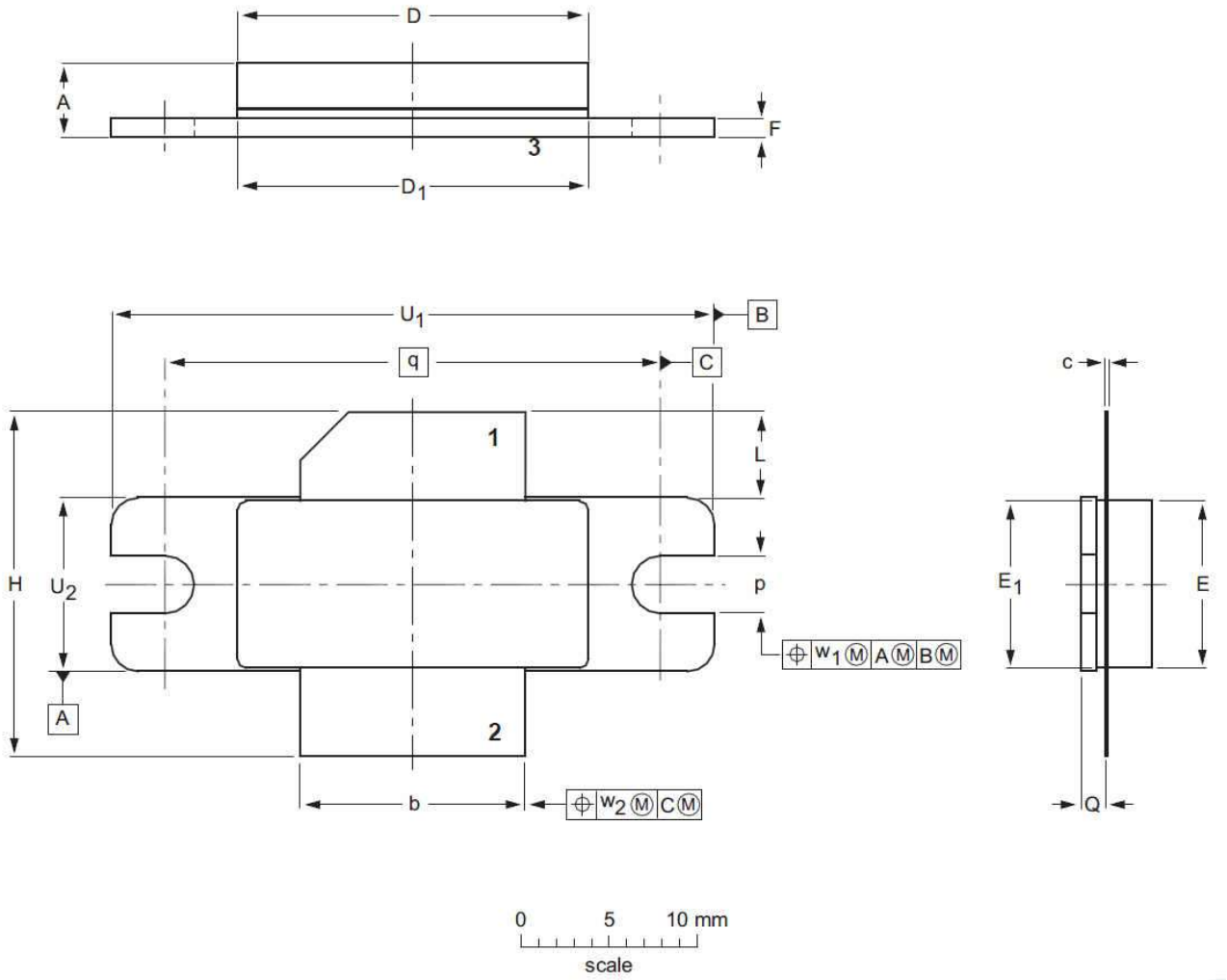


Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.3pF	0805	1
C2, C3, C4	33pF	0805	3
C5, C6, C7, C8, C9, C10, C11, C12, C15	3.9pF	0603	9
C13, C14, C16,	2.0pF	0603	3
C17, C18	10uF/100V	1210	2
C19	220uF/63V		1
R1	10ohm	0603	1

Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/3/3	Rev 1.0	Preliminary datasheet
2023/3/20	Rev 2.0	Rated P1dB increased to 150W

Application data based on LSM-21-06

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