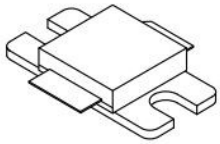
MG1509V LDMOS TRANSISTOR

Document Number: MG1509V
Preliminary Datasheet V1.0

90W, 0.96-1.4GHz 50V High Power RF LDMOS

MG1509V



Description

The MG1509V is a 90W single ended 50V LDMOS, internally matched for any applications within 0.96-1.4GHz

It is suitable for avionics application of 960-1215MHz, and L band application of 1200-1400MHz.

- Typical performance(on 960-1215MHz application board with devices soldered)

MG1509VS VDS=50V IDQ=20mA VGS=3.17V pulse							Harmonics (Pout=Psat)	
F (MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	I (A)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc)
960	35.5	49.8	95.5	0.37	14.3	56.8	22	35
1000	35.5	49.8	94.8	0.39	14.3	53.4	22.8	46
1050	35.5	50.1	102.3	0.41	14.6	54.7	25.5	24.1
1100	35.6	50	100	0.40	14.4	54.8	25.6	37.6
1150	35.7	49.9	98.2	0.4	14.2	53.8	25.7	54
1215	35.6	50.1	103.3	0.42	14.5	53.8	25.6	60

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 C, 90 W Peak, 100usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1030 MHz	$R_{\theta JC}$	0.4	°C/W

3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

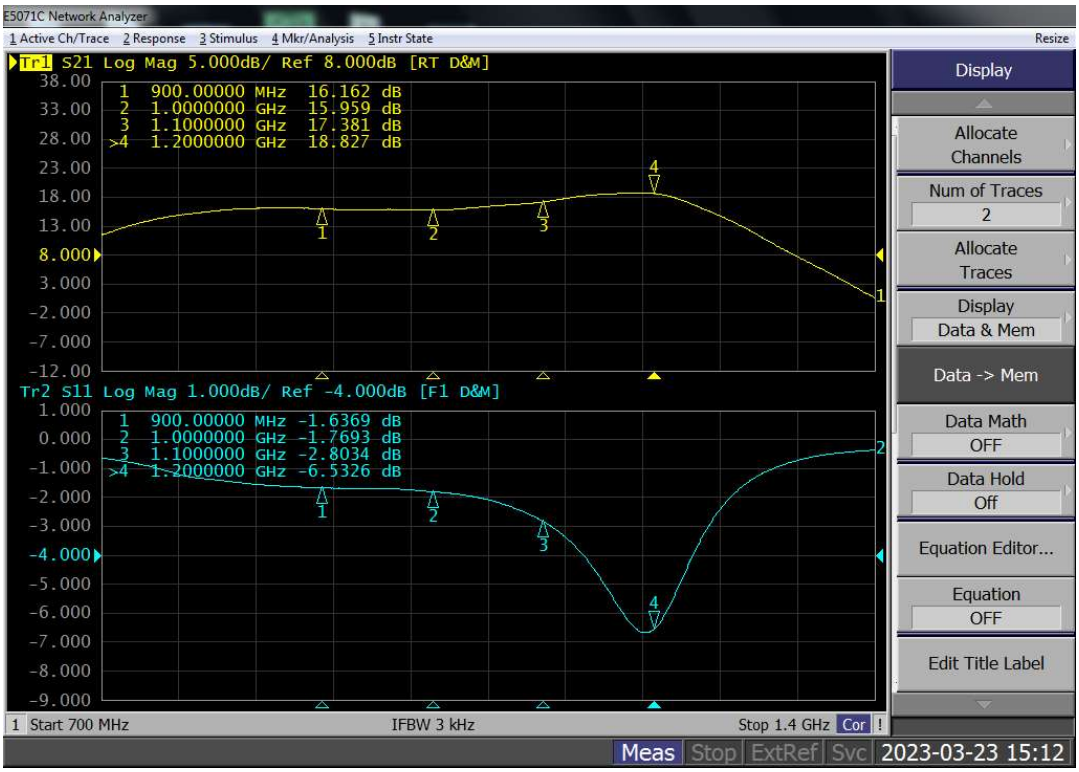
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.37		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200mA, f = 1030MHz, pulse width:100us, duty cycle:10%, Pout=90W

VSWR: > 7:1 at All Phase Angles	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 2: Network analyzer output S11/S21 at 50V Idq=200mA



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

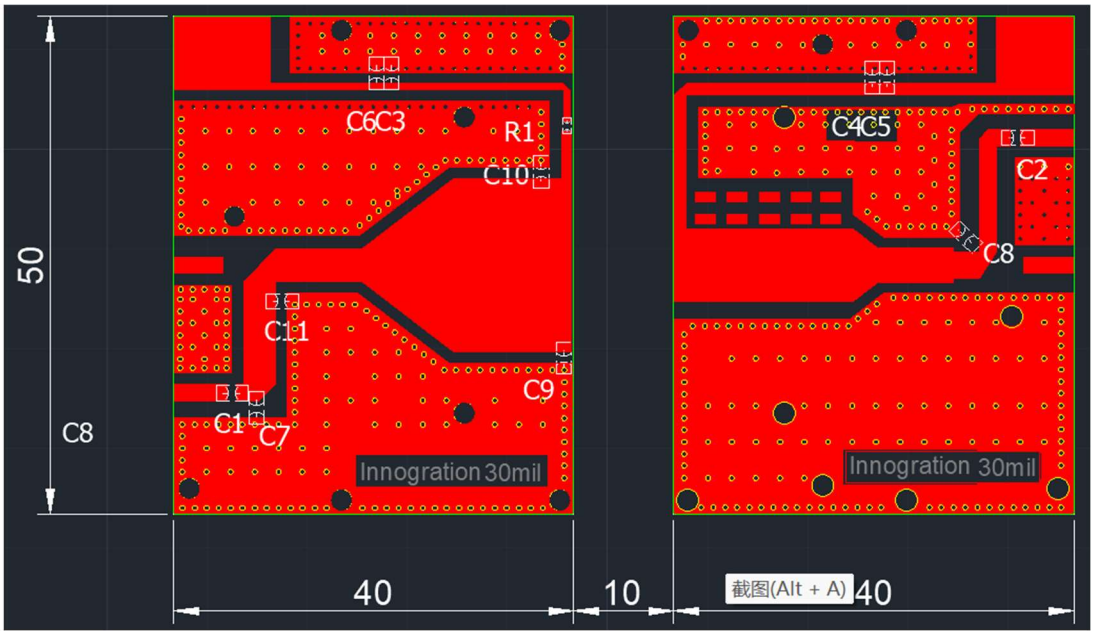
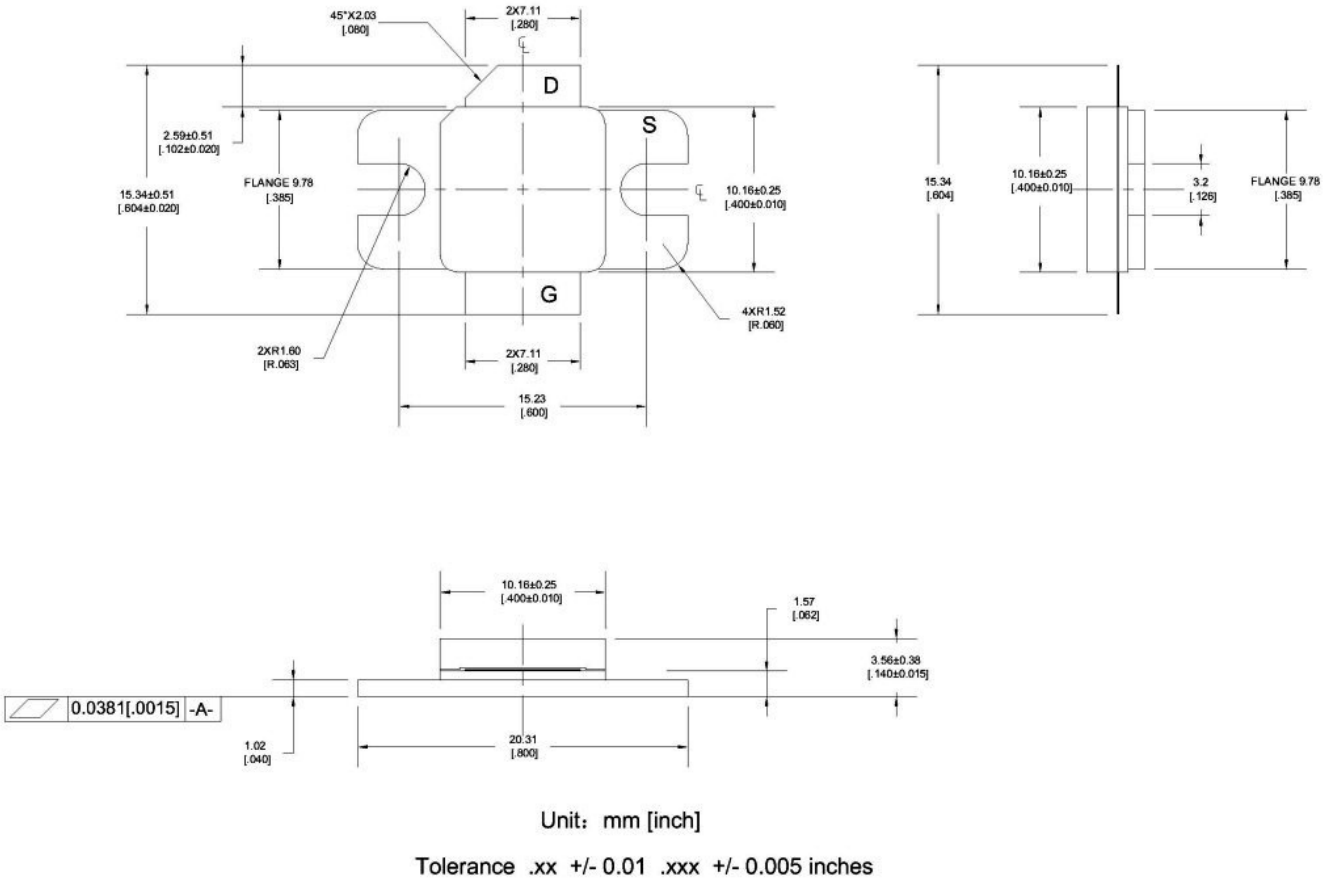


Table 5. Test Circuit Component Designations and Values

Part	description	Model
R1	8.20Ω	Chip Resisto
C1,C2,C3,C4	68pF MQ10111	
C5,C6	10uF 1210	
C7,C8	2.4pF MQ10111	
C9	6.8pF MQ10111	
C10	2.0pF MQ10111	
C11	1.8pF MQ10111	
PCB	30mil Rogers4350B	

Package Outline

Eared Flanged ceramic package; 2 leads



Unit：mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/3/23	Rev 1.0	Preliminary datasheet

Application data based on SYX-23-09

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