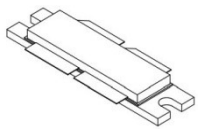
M2Q1060RVP LDMOS TRANSISTOR

Document Number: M2Q1060RVP
Preliminary Datasheet V1.0

600W, HF-0.9GHz 50V High Power RF LDMOS FETs

M2Q1060RVP



Description

The M2Q1060RVP is a 600W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications from HF up to 900MHz, supporting both pulse and CW applications.

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as VHF communication, UHF TV and Aerospace applications.

There isn't guarantee when this device is used outside of the band stated above.

- Application data at various frequencies(Vgs=3.2V,Vds=50V, Idq=140mA)

Frequency(MHz)	Signal	Pin(dBm)	Poutt(W)	Gain(dB)	Eff(%)
225	CW	36	600	22	72
700-900	Pulse	44	520-640	13~14	>50~60

Features

- High breakdown voltage enable high ruggedness
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 600W CW, 50 Vdc, I_{DQ} = 140 mA	$R_{\theta JC}$	0.27	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 50V, V_{GS} = 0 V)					
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 140 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.05	——	V

TYPICAL CHARACTERISTICS (700-900MHz)

M2Q1060RVP^{V0} V_{DS}=50V V_{GS}=3.04V I_{DQ}=140mA Pulse Width 12us 50%

Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2nd Harmonic (dBc)	3rd Harmonic (dBc)
700	57.99	629.5	10.31	43.15	14.84	61.06	-33	-41.3
750	57.66	583.4	10.66	43.30	14.36	54.73	-34.2	-35.3
800	57.79	601.2	11.81	44.04	13.75	50.90	-40.7	-42.9
850	58.11	647.1	11.78	44.21	13.90	54.94	-44.8	-52.6
900	57.19	523.6	9.03	43.77	13.42	57.98	-44.1	-52.7

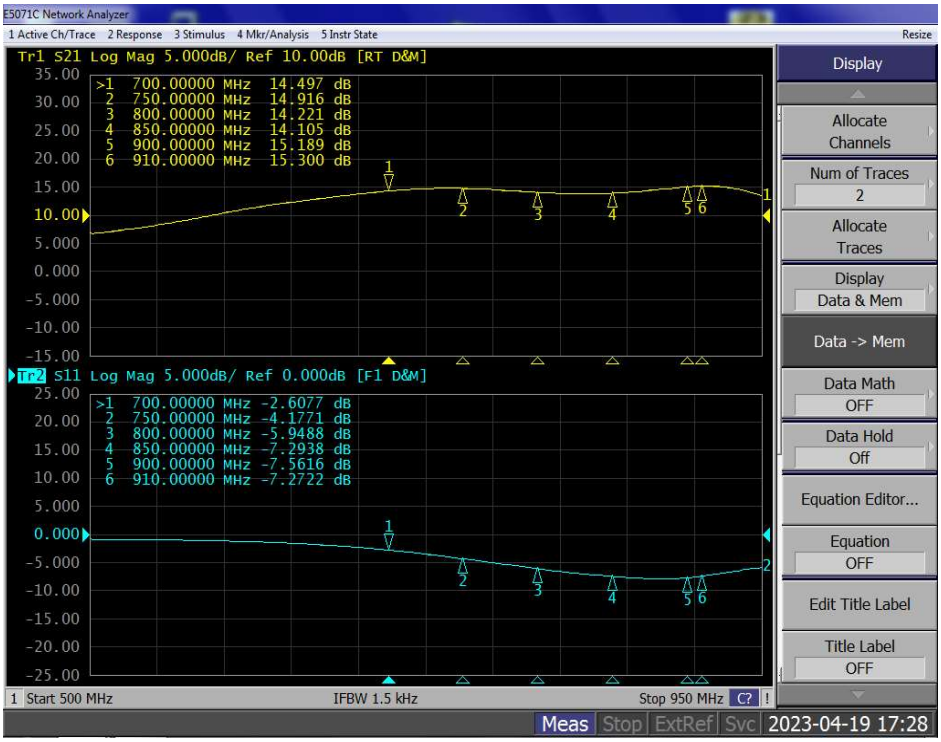
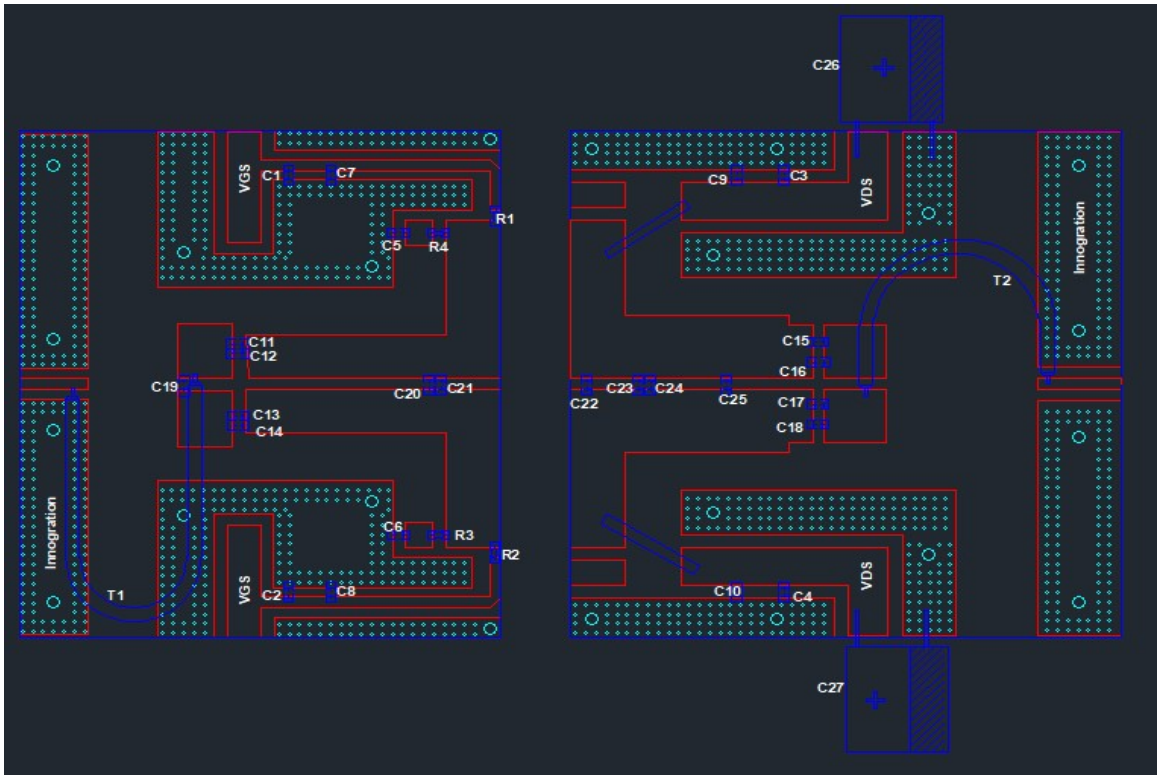


Figure 1: Network analyzer output, S11 (Vds=50V,Idq=340mA, Vgs=3.2V)

Reference Circuit of Test Fixture (700-900MHz)

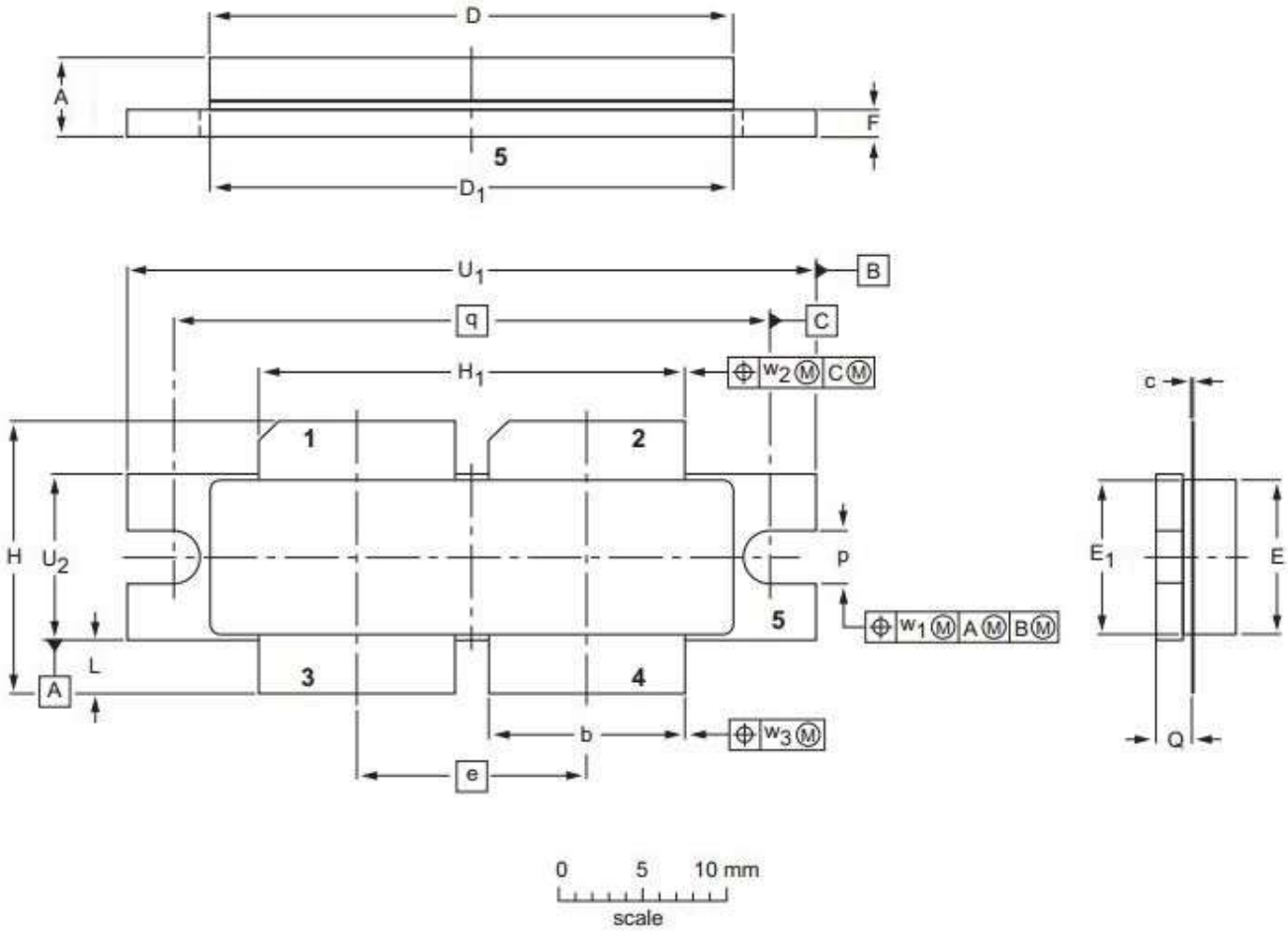
(Layout file upon request) PCB: Roger 4350B, 30mils



Component	Description	Suggestion
C1~C6	10uF	10uF/100V
C7~C10	200pF	MQ101111
C11~C14	27pF	MQ101111
C115~C18	18pF	MQ101111
C19	3pF	MQ101111
C20	12pF	MQ101111
C21,C24	6.8pF	MQ101111
C22	5.1pF	MQ101111
C23	3.9pF	MQ101111
C25	6.2pF	MQ101111
C26,C27	4700uF/63V	Electrolytic Capacitor
R1,R2	51 Ω	Chip Resistor
R2,R3	10 Ω	Chip Resistor
T1	50ohm,45mm	RFSFBU-086-50
T2	25 Ohm ,55mm	SFF-25-1.5

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/4/20	Rev 1.0	Preliminary Datasheet

Application data based on TC-23-19

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