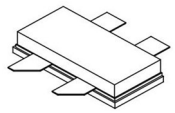
GaN HEMT 50V, 600W,1.3-1.6GHz RF Power Transistor

Description

STBV15600BY4



The STBV15600BY4 is a dual path 600watt , Input matched GaN HEMT, ideal for applications from 1.3 to 1.6GHz especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=250mA(Vgm=-3.31V，Vgp=-5.30V)

Pulsed CW: 20uS width, 10% cycle.

Freq (MHz)	Pulse CW Signal(1)				P_{avg}=50dBm WCDMA Signal(2)		
	P3 (dBm)	P3 Eff (%)	P5 (dBm)	P5 Eff (%)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
1365	575.25	71.55	632.98	70.66	17.02	57.47	-30.93
1445	539.80	71.59	674.35	74.40	17.44	59.67	-31.29
1525	618.30	78.50	637.69	79.49	16.40	56.41	-31.55

Applications

- Asymmetrical Doherty amplifier within 1.3-1.6GHz
- L band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

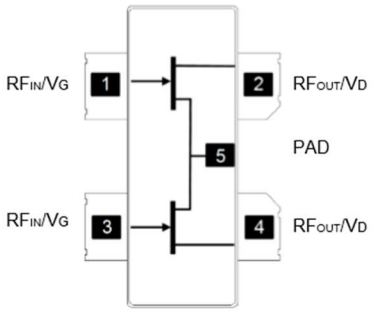


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	83	mA

Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=90W, on Doherty application board	$R_{\theta JC}$	0.85	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=36mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 36mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.24		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=47mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 47mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.5GHz, Pout=90W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

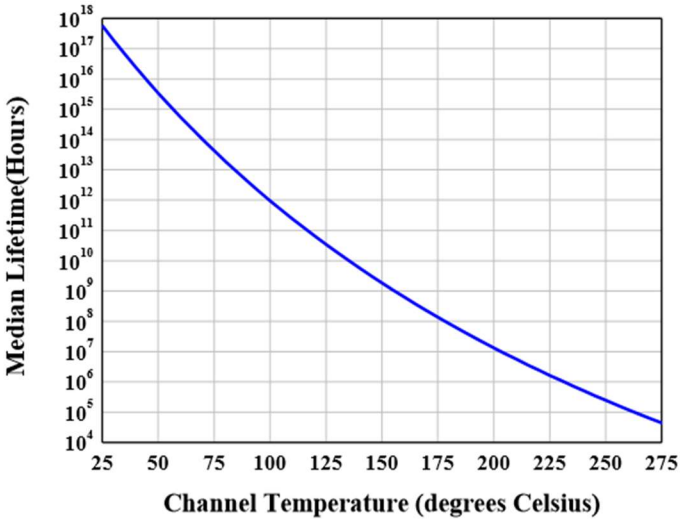


Figure 3: Efficiency and power gain as function of Pout

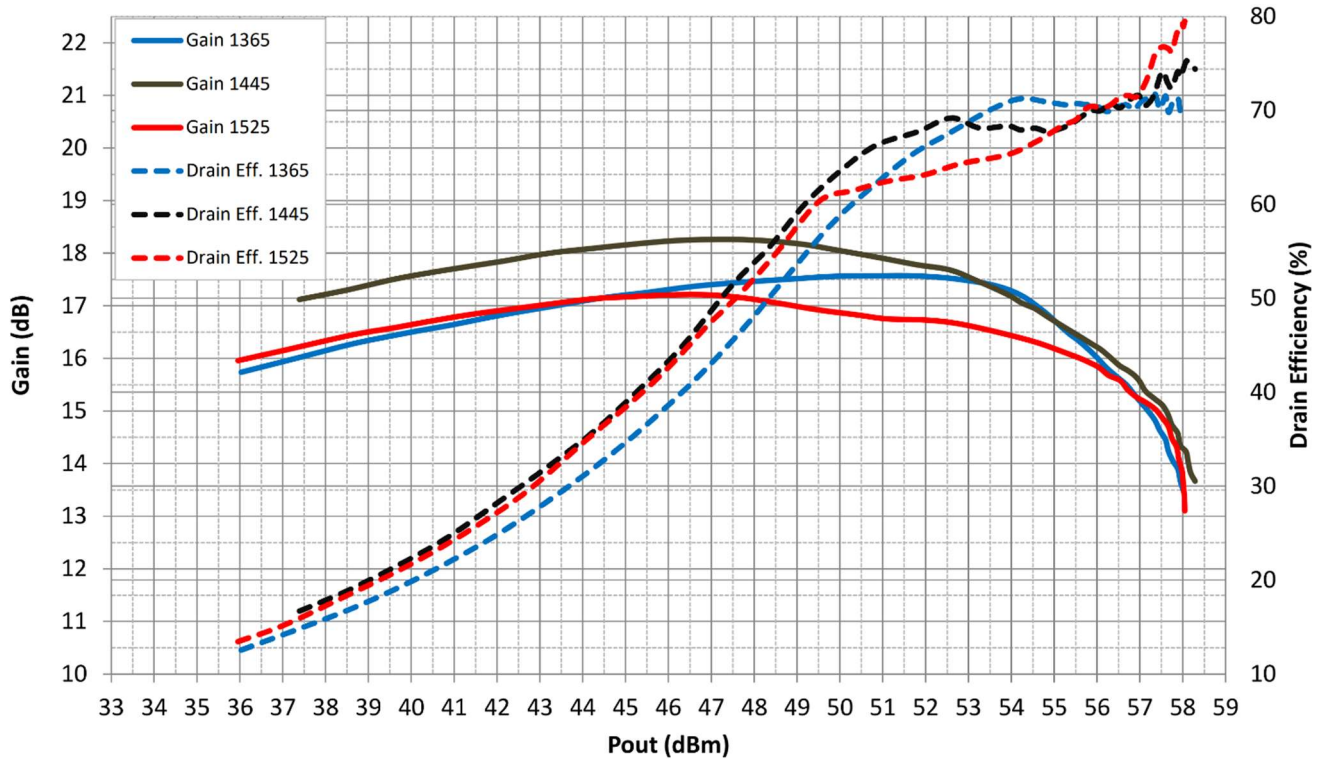


Figure 4: Network analyzer output, S11 and S21

m1	m2	m3
freq=1.365 GHz	freq=1.445 GHz	freq=1.525 GHz
dB(S(2,1))=17.029	dB(S(2,1))=18.098	dB(S(2,1))=17.202
dB(S(1,1))=-16.168	dB(S(1,1))=-16.693	dB(S(1,1))=-14.403

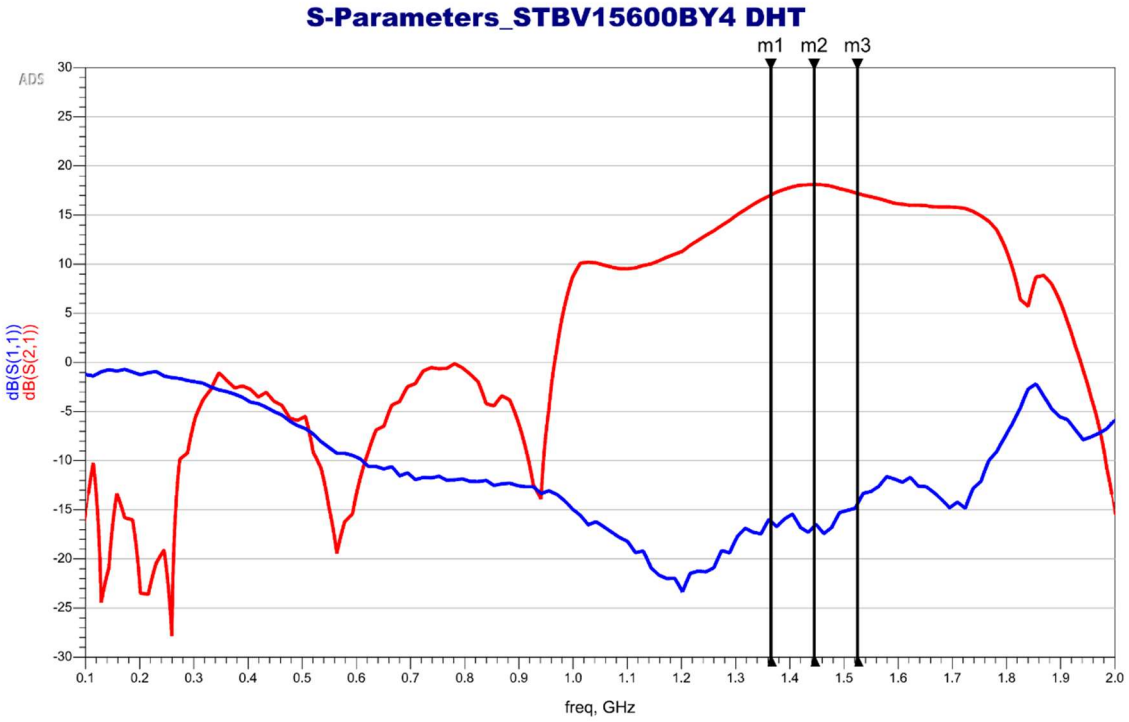


Figure 5: Picture of application board Doherty circuit

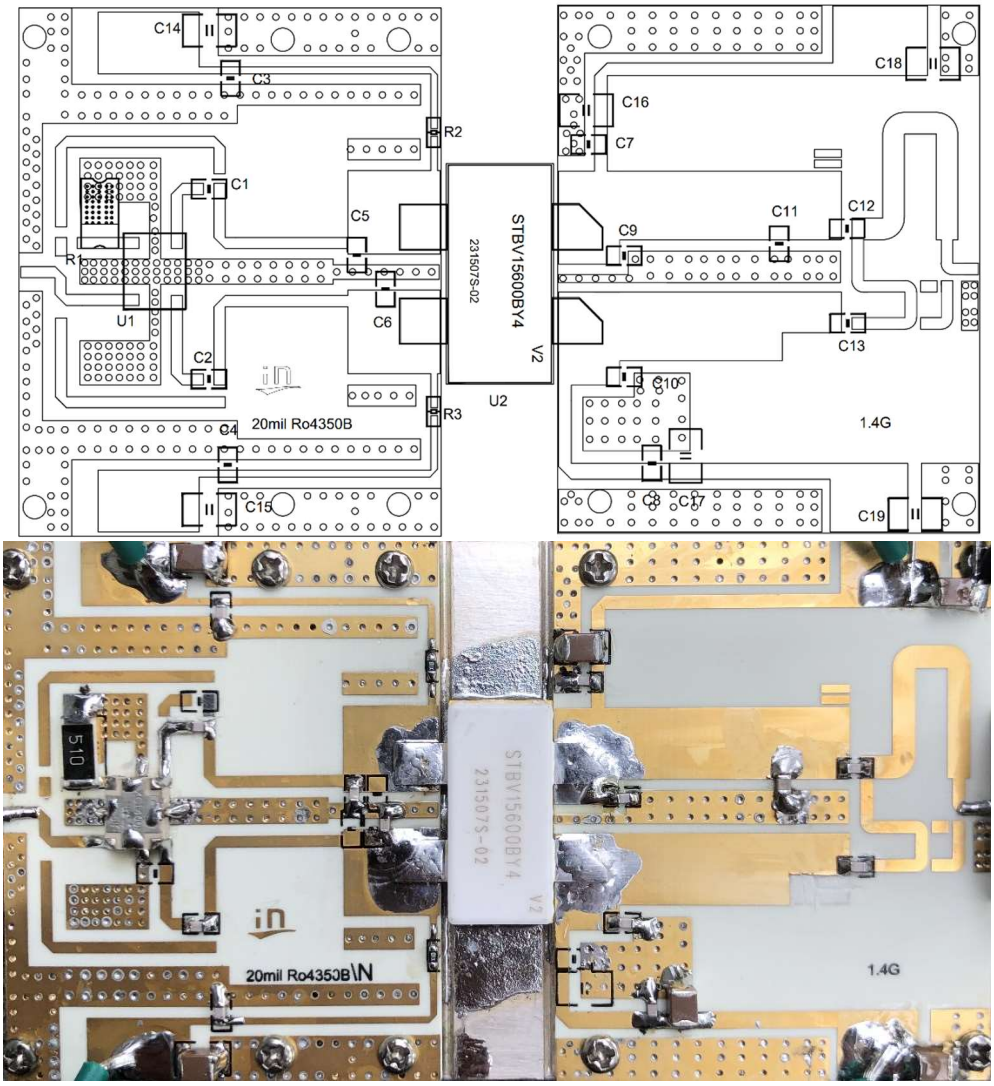
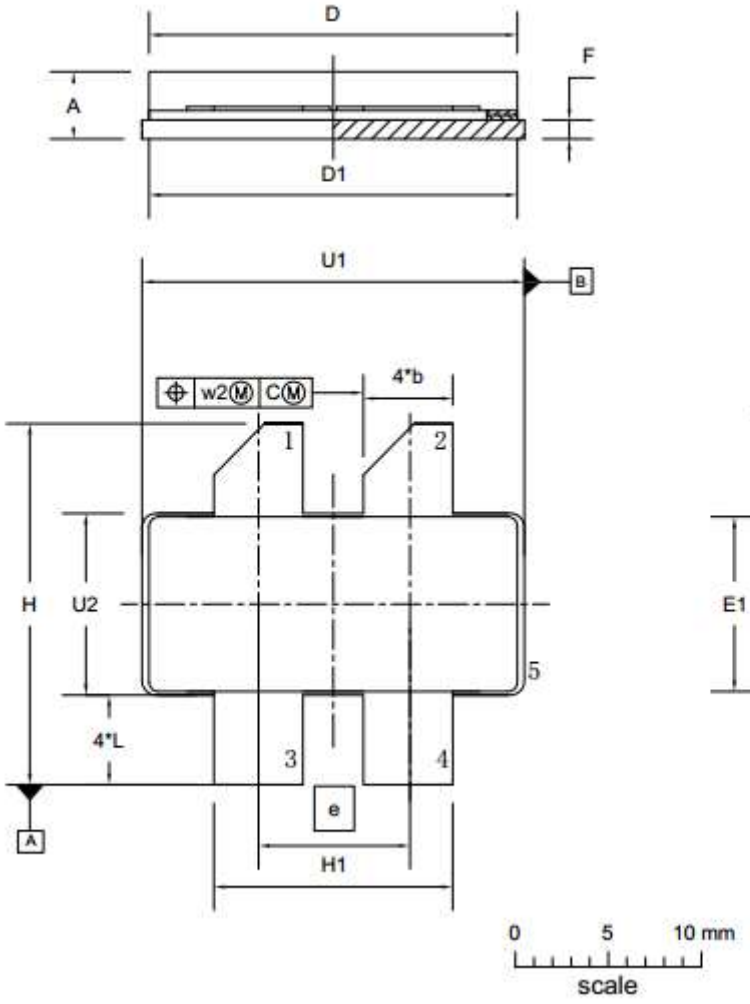


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C7, C8, C13	0603	33pF/250V	7
C5, C12	0603	3.9pF/250V	2
C6, C10	0603	4.7pF/250V	2
C9	0603	6.8pF/250V	2
C11	0603	0.2pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
R2, R3	0603	10R	2
R1	2512	51R	1
U1	6.35*5.08mm	XC1400P-03S	1
U2	BY4	STBV15600BY4	1

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/4/25	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: ZBB-23-15

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