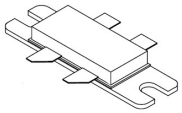
M2K1026VP LDMOS TRANSISTOR

Document Number: M2K1026VP
Preliminary Datasheet V1.1

260W, 50V High Power RF LDMOS FETs

M2K1026VP



Description

The M2K1026VP is a 260-watt, highly rugged, thermally enhanced, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.0 GHz. In its typical broadband application, it can deliver >200W CW across the full band of 30-1000MHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical Performance (On Innogration 30-1000MHz broad band fixture with device soldered):

M2K1026VPS^{V0} Vds=50V Vgs=3.11V Idq=120mA CW								
Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff(%)	2nd (dBc)	3rd (dBc）
30	54.91	309	12.41	39.26	15.65	49.92	-30.2	-10.0
100	55.60	363	12.18	38.65	16.95	59.62	-37.0	-10.2
200	55.18	329	12.65	38.83	16.35	52.11	-44.8	-10.8
300	55.09	322	12.40	37.58	17.51	52.07	-45.5	-12.0
400	55.30	338	12.53	36.15	19.15	54.09	-40.7	-14.7
500	55.05	319	12.00	36.20	18.85	53.31	-45.7	-34.6
600	54.30	269	11.03	35.31	18.99	48.80	-33.2	-28.6
700	54.28	267	11.90	36.07	18.21	45.03	-55.4	-25.2
800	54.30	269	11.60	38.60	15.70	46.41	-54.7	-37.2
900	53.87	243	11.00	40.22	13.65	44.32	-45.6	-39.0
1000	53.53	225	9.15	38.71	14.82	49.27	-39.1	-30.0

When used at lower voltage like 40V, it can delivery >150W CW across the band, with more thermal margin

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 25°C, DC Test	RθJC	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics(Half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$	105	110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.16	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		900		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		85		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		36		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.2		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 200mA, f = 915 MHz, Pulsed CW Signal Measurements, Pin=34dBm

Power Gain@Pout	Gp	——	19	——	dB

Output Power	Pout		260		W
Drain Efficiency@Pout	η_D	——	60	——	%
Input Return Loss	IRL	——	-7	——	dB
Ruggedness at all phase angle	VSWR		10:1		

TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21

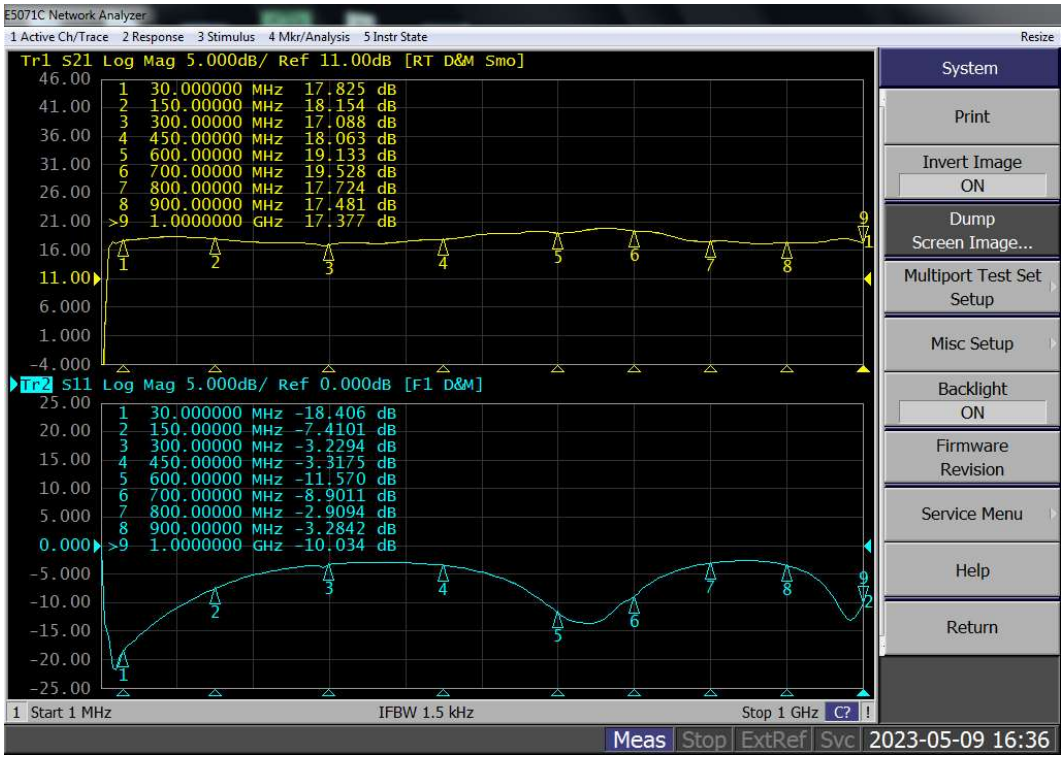
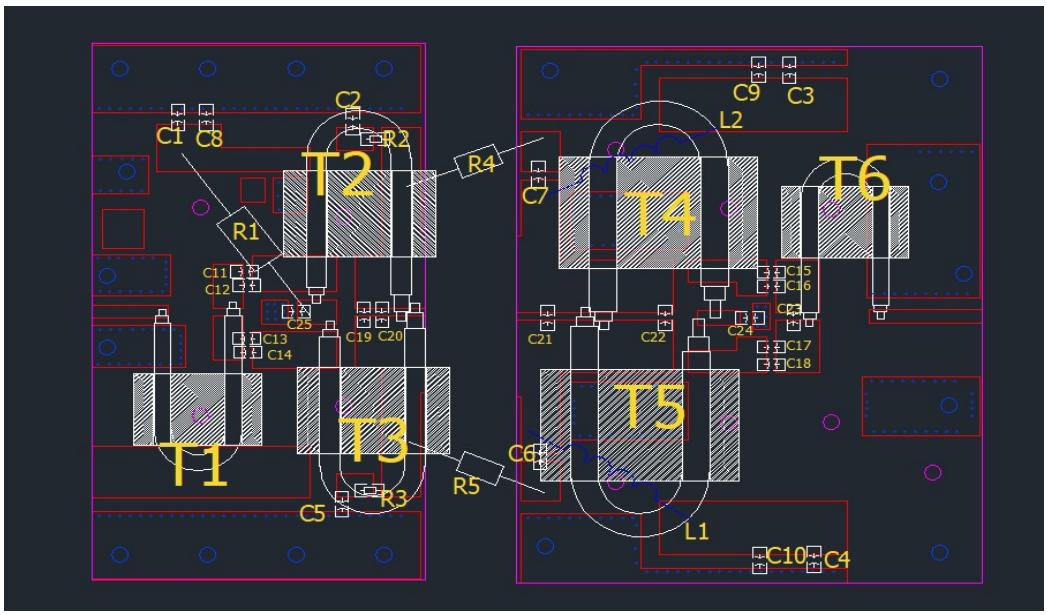


Figure 2. Test Circuit Component Layout

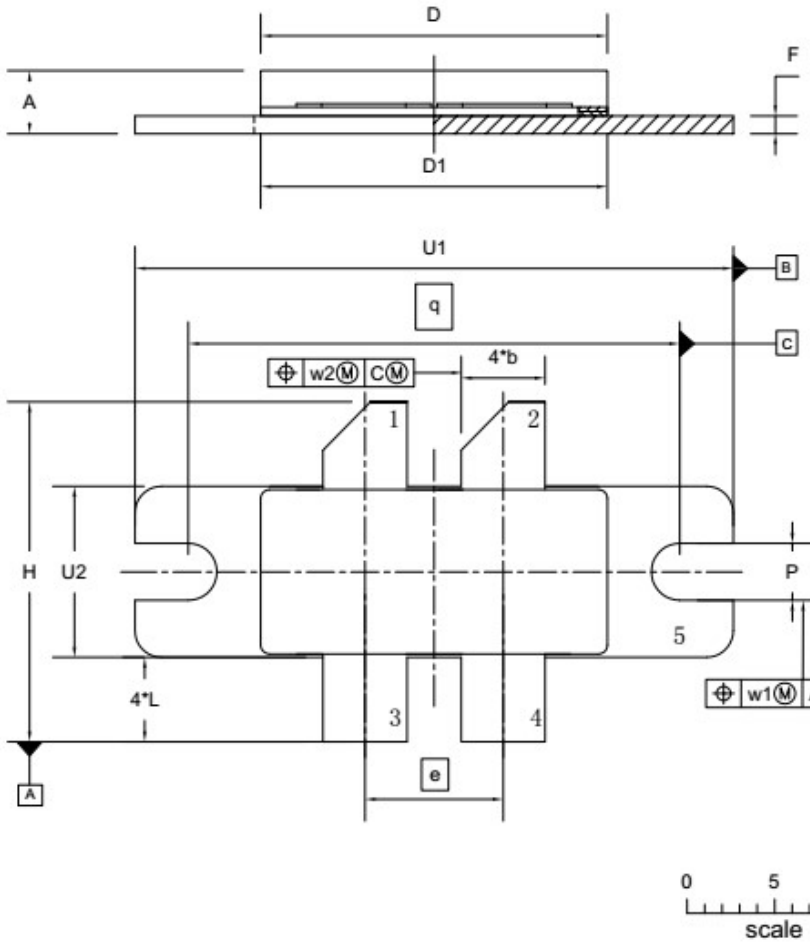
(PCB Roger 4350B 30Mil, PCB file upon request)



Component	Description	Suggestion
C1~C7	10uF	10uF/100V
C8~C18	470pF	MQ101111
C19	8.2pF	MQ101111
C20	10pF	MQ101111
C21	2pF	MQ101111
C22	4.3pF	MQ101111
C23	1.5pF	MQ101111
C24	560pF	MQ101111
C25	360pF	MQ101111
R2,R3	10 Ω	Chip Resistor
R1,R4,R5	330 Ω	
L1,L2	8turns	DIY air core inductance
T1	50ohm,70mm	RFSFBU-086-50,BN-61-202
T2,T3	12.5ohm,70mm	SFF-12.5-1.5,BN-61-202
T4,T5	16.7 ohm ,70mm	SFF-16.7-1.5,BN-61-202
T6	50ohm,60mm	RFSFBU-086-50,BN-61-202

Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/10	Rev 1.0	Preliminary Datasheet Creation
2023/7/14	Rev 1.1	Modify the typo of breakdown voltage

Application data based on TC-23-25

Disclaimers