



# GaN 50V, 500W, 2.45GHz RF Power Transistor

**STCV25500BY2**

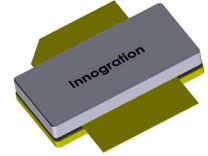
## Description

The STCV25500BY2 is a single ended 500watt capable, GaN HEMT, ideal for ISM applications **at the narrower sub-band within 2.4-2.5GHz**

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at **2.44-2.46GHz** applications

$V_{DD} = 50 \text{ Vdc}$ ,  $V_{GS} = -3.35\text{V}$ ,  $I_{dq} = 120\text{mA}$ , with device soldered



### CW:

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	Gain(dB)	Eff(%)
2440	41.0	57.6	575	16.6	72
2450	41.2	57.47	550	16.3	72
2460	41.2	57.20	525	16.0	71

Recommended driver: STAV58016P2

## Applications

- 2.45GHz RF Energy
- S band power amplifier

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set  $V_{GS}$  to the pinch-off ( $V_P$ ) voltage, typically  $-5 \text{ V}$
2. Turn on  $V_{DS}$  to nominal supply voltage
3. Increase  $V_{GS}$  until  $I_{DS}$  current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce  $V_{GS}$  down to  $V_P$ , typically  $-5 \text{ V}$
3. Reduce  $V_{DS}$  down to  $0 \text{ V}$
4. Turn off  $V_{GS}$

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to +0.5	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum gate current	$I_{GS}$	51	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$ , at $P_d = 200\text{W}$	$R_{\theta JC}$	0.6	°C /W

**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

#### DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 68\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 68\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 120\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.3		V



**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=500W pulse CW All phase, No device damages	VSWR		5:1		

**TYPICAL CHARACTERISTICS**

Figure 2: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.26V)

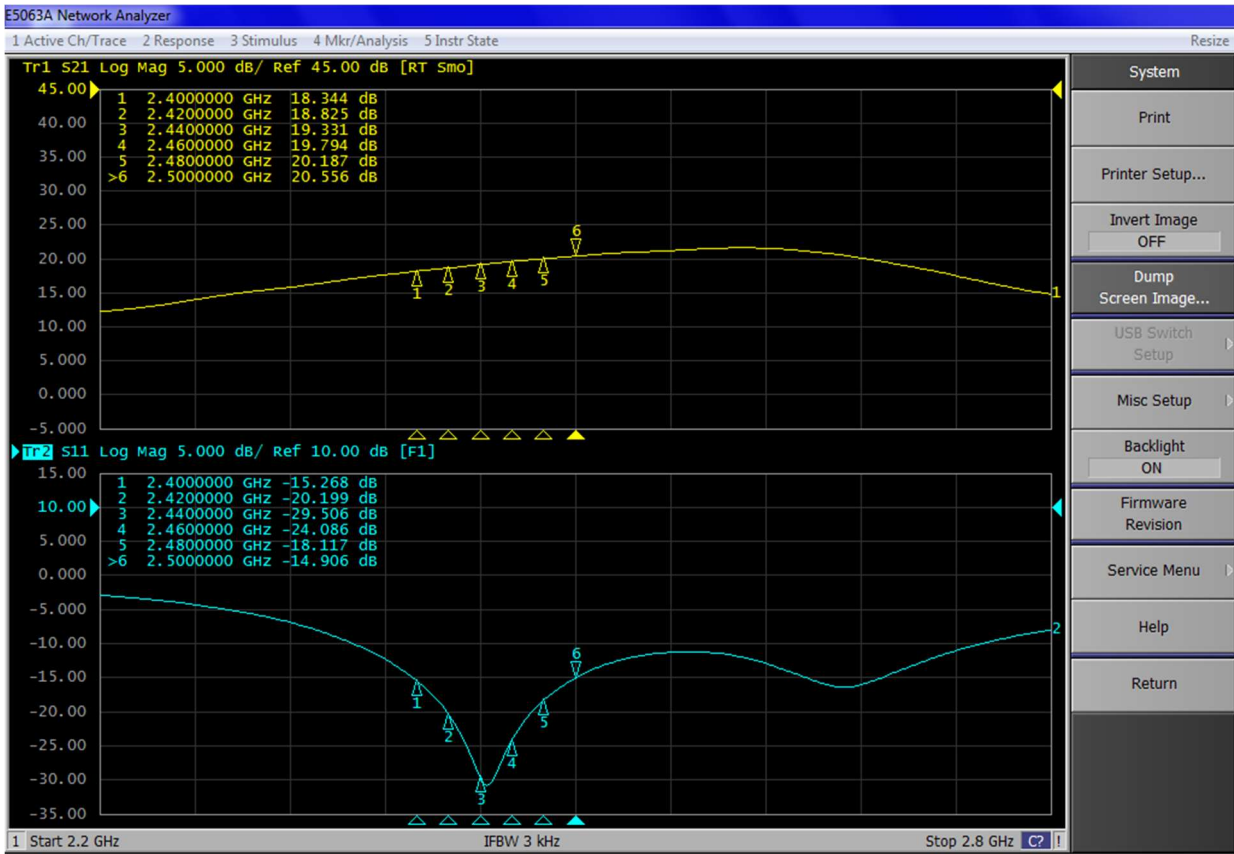
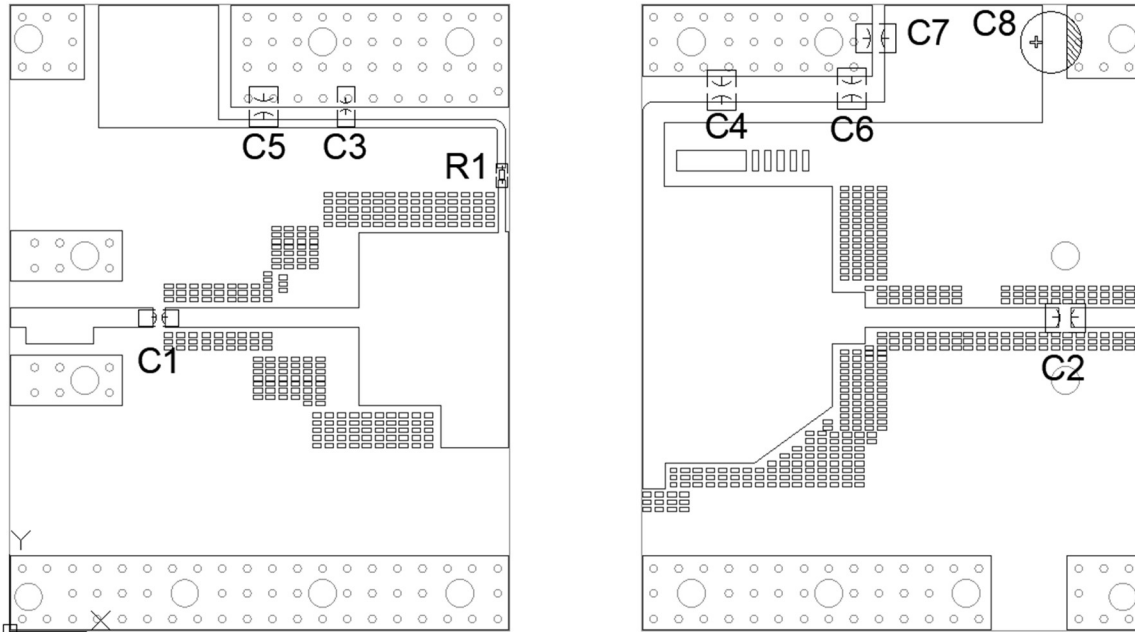


Figure 3: Reference design circuit (PCB DWG file upon request,)

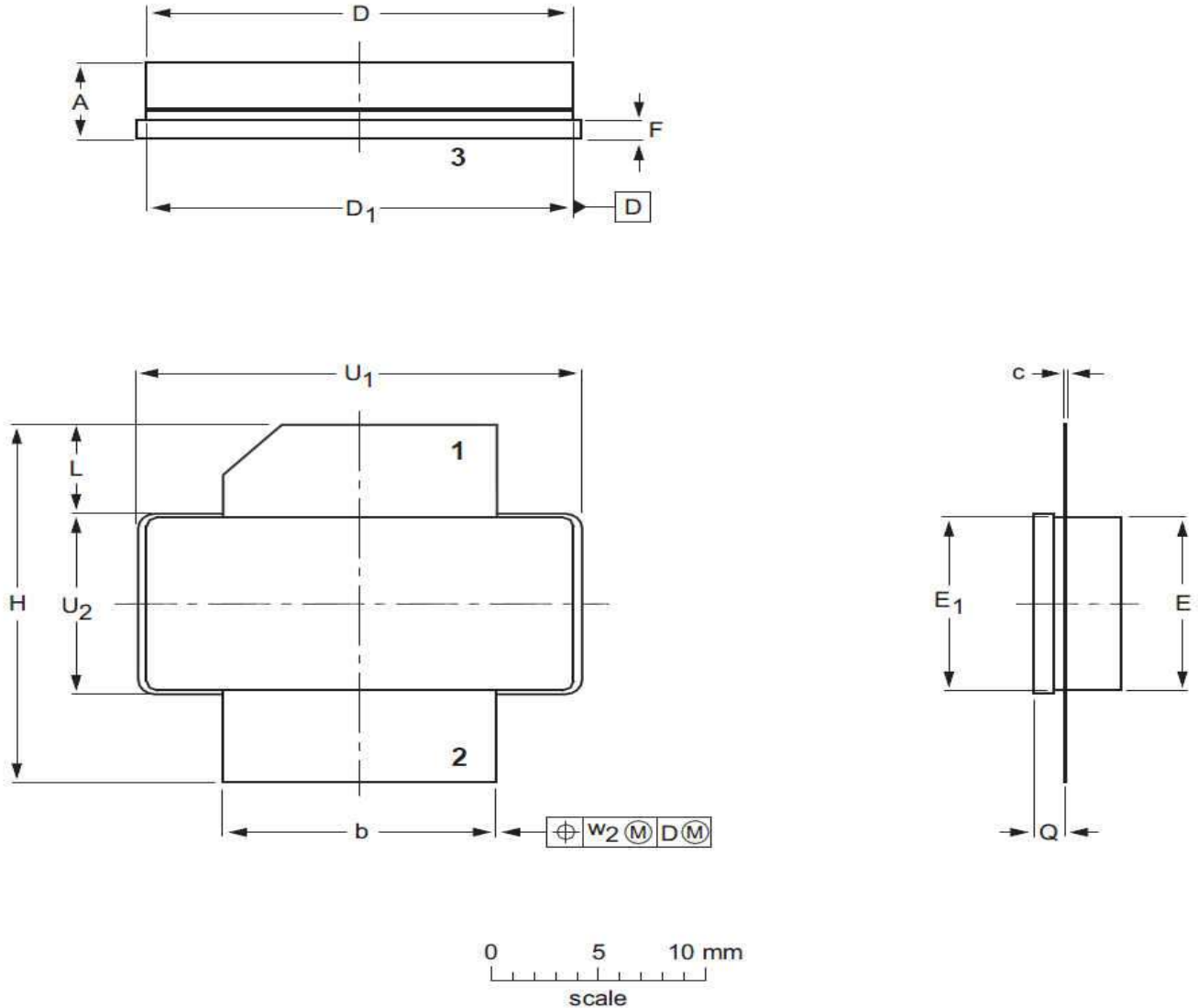


Component	Description	Suggestion
C1,C3	18pF	MQ200805C0G2E150JNDB
C2	15pF*3	ATC800B
C4	15pF	ATC800B
C5,C6,C7	Ceramic multilayer capacitor, 10uF, 100V	1210
C8	4700uF/63V	
R1	Chip Resistor, 10 $\Omega$	0805
PCB	board material: Rogers tc350-plus, $\epsilon_r = 3.5$ , thickness 30 mils, 1oz copper on each side	



### Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/12/25	V1.0	Preliminary Datasheet Creation

Application data based on: YHG-22-31

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