



GaN 50V,800W, RF Power Transistor

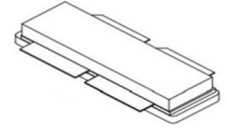
SQ1080RVPS

Description

The SQ1080RVPS is a push pull 800W capable, internally matched GaN HEMT, ideal for multiple applications up to 1GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 700 to 910MHz, it can deliver >600W across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.



- Typical Pulsed CW performance at 700-910MHz applications

SQ1080RVPS ^{V0} Vgs=-3.25V Vds=50V Idq=100mA Pulse 12us 50%						
Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)
700	58.40	691.8	10.30	41.10	17.30	67.17
750	57.89	615.2	9.98	41.61	16.28	61.64
800	58.02	633.9	10.00	40.56	17.46	63.39
850	57.91	618.0	9.90	41.10	16.81	62.43
910	58.04	636.8	9.97	42.37	15.67	63.87

Applications

- P band power amplifier
- UHF TV
- Public Safety Radio
- Data link power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	I _{gs}	100	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C



Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 25^\circ\text{C}$, at $P_{out} = 600\text{W}$ @ 900MHz	$R_{\theta JC}$	0.22	°C /W

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

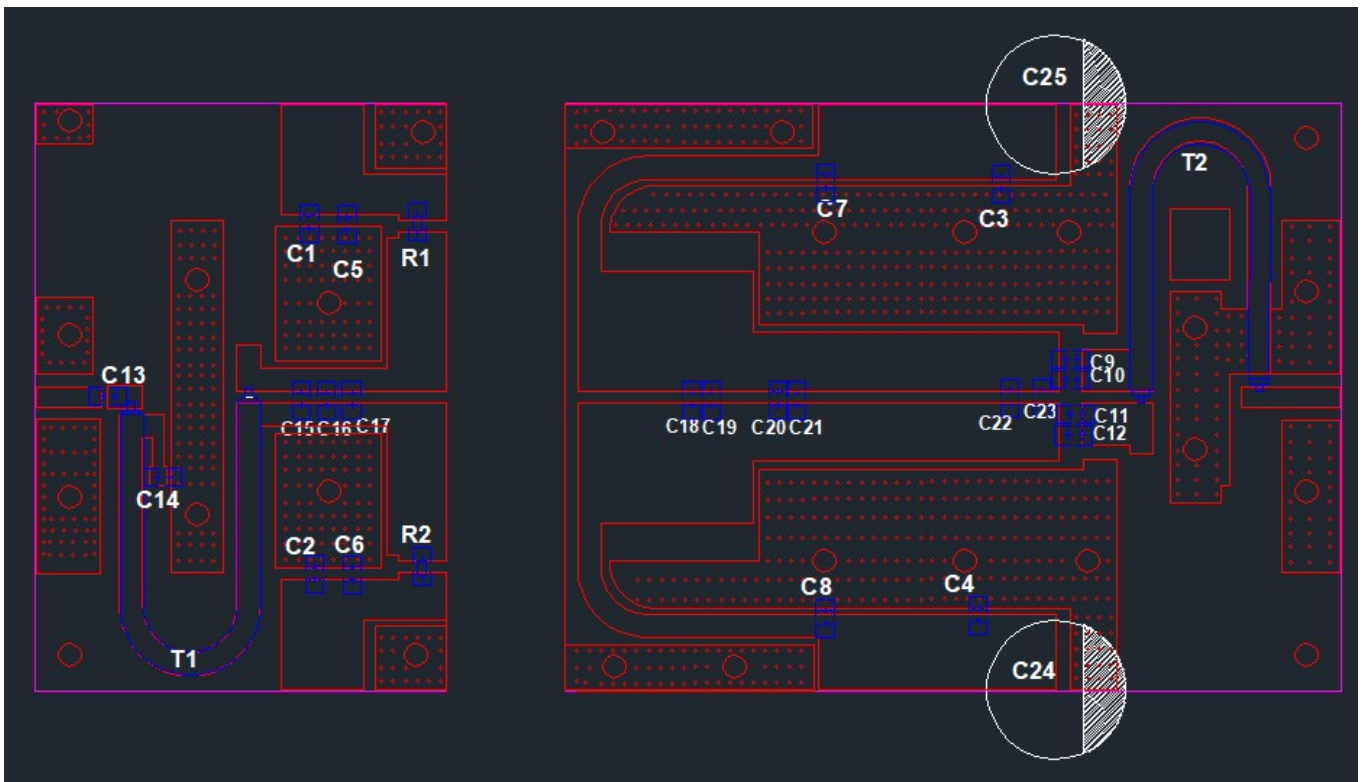
DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 100\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 100\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 180\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

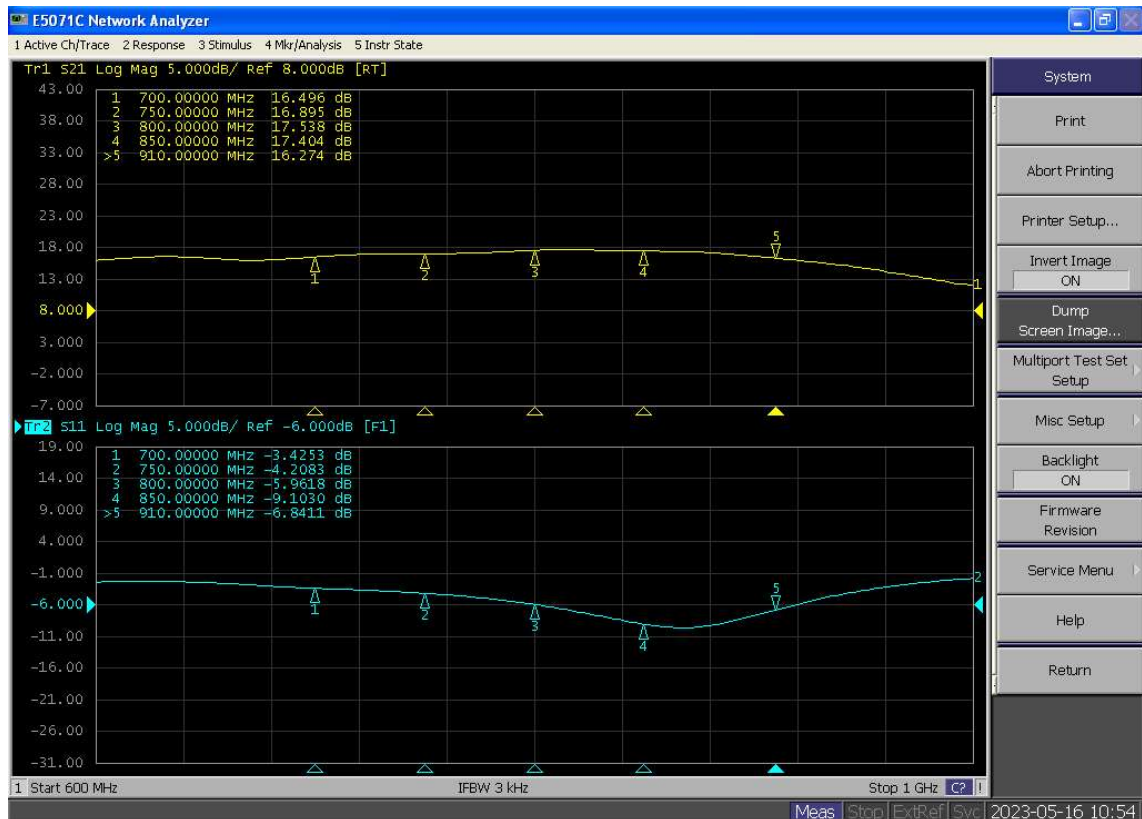
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, $P_{out} = 600\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

Figure 1: Reference design circuit (PCB DWG file upon request,)





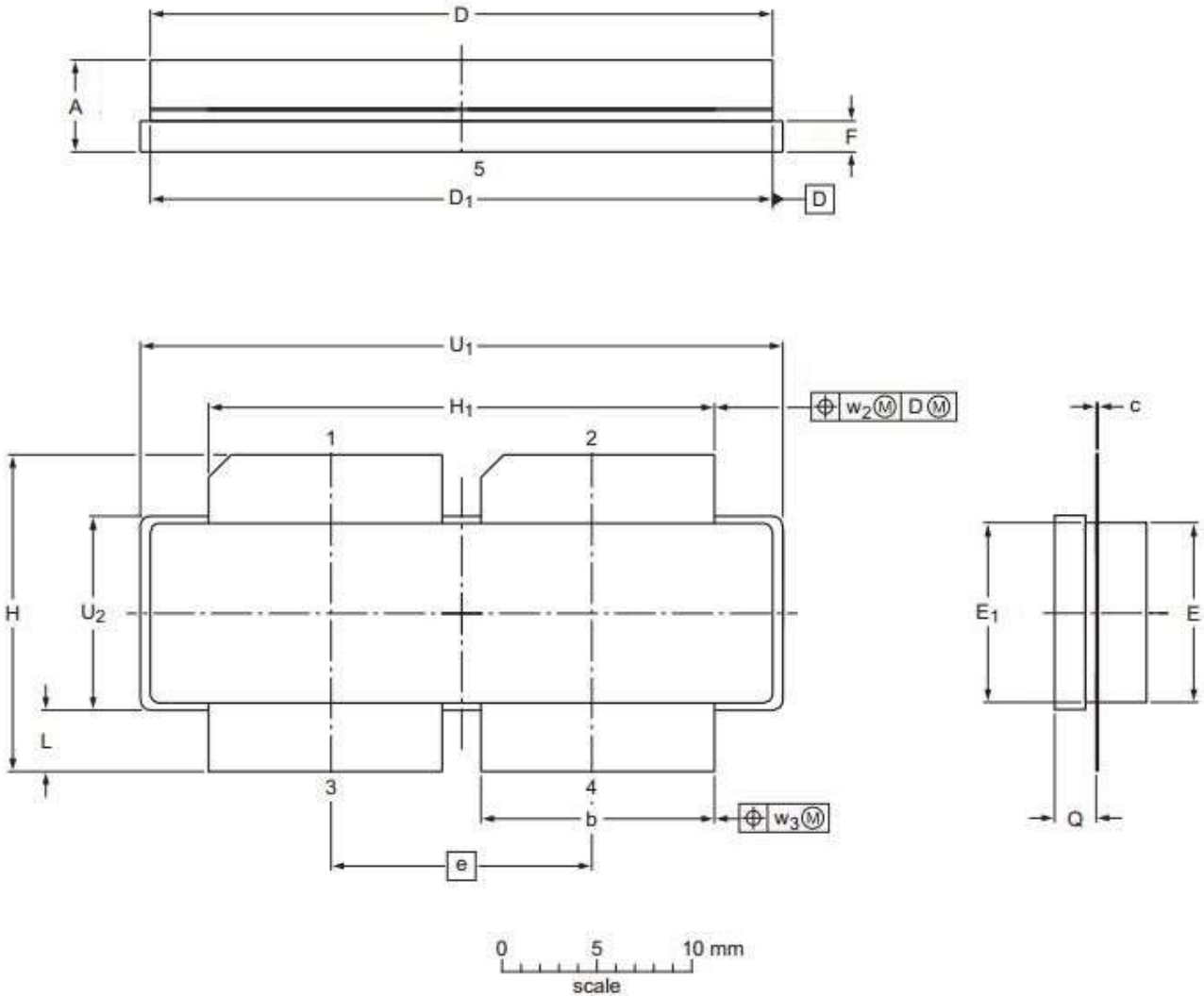
Component	Description	Suggested Manufacturer
C1,C2,C3,C4	10uF	10uF/100V
C5,C6	39pF	MQ101111
C7,C8	150pF	MQ101111
C9,C10,C11,C12	20pF	MQ101111
C13	33pF	MQ101111
C14	47pF	MQ101111
C15,C18,C21	5.1pF	MQ101111
C16	12pF	MQ101111
C17	10pF	MQ101111
C19,C22,C23	1pF	MQ101111
C20	4.3pF	MQ101111
C24,C25	4700uF/50V	Electrolytic Capacitor
R1,R2	18 Ω	Chip Resistor
T1	25 ohm,55mm	RFSFBU-086-25
T2	35 ohm ,55mm	SFF-35-3
PCB	30Mil Rogers4350	





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/23	V1.0	Preliminary Datasheet Creation

Application data based on:TC-23-28

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