

# MG3503S LDMOS TRANSISTOR

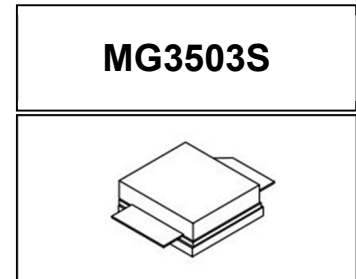
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Product Datasheet V1.0

## 40W, 2.5-3.5GHz 28V RF LDMOS FETs

### Description

The MG3503S is a 40-watt, internally matched, single ended LDMOS FETs, designed for multiple applications within full band 2.5-3.5GHz.

It can be used in Class AB/B and Class C for all typical modulation formats, for CW and pulsed, linear or saturated applications.



- Typical Performance (On Innogration **2.5-3.5GHz** fixture with device soldered):

MG3503S Vds=28V,Vgs=2.51V,Idq=50mA Pulse:100us,10%						
Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	Ids(A)	Gain(dB)	Eff(%)
2500	37.29	46.90	49.0	0.47	9.6	47.3
2700	37.34	47.09	51.2	0.52	9.8	43.5
2900	37.28	46.99	50.0	0.52	9.7	39.8
3100	37.54	47.37	54.6	0.57	9.8	41.5
3300	37.21	47.16	52.0	0.54	10.0	42.2
3500	37.52	47.41	55.1	0.49	9.9	50.4

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- S band amplifier
- ISM applications
- Cellular amplifier

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+65	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+32	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>j</sub>	+225	°C

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**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , DC test	$R_{\theta JC}$	1.3	$^\circ\text{C/W}$

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**DC Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$			100	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$			1	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 10\text{V}$ , $V_{DS} = 0\text{V}$ )	$I_{DSS}$			1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 28\text{V}$ , $I_D = 450\mu\text{A}$ )	$V_{GS(th)}$		2.0		V
Gate Quiescent Voltage ( $V_{DD} = 28\text{V}$ , $I_D = 50\text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$		2.4		V

**Functional Tests** (On Demo Test Fixture, 50 ohm system)  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 50\text{mA}$ ,  $f = 2500\text{--}3500\text{MHz}$ , Pulse CW Signal .

Power Gain	$G_p$	9.5			dB
Drain Efficiency@P3dB	$\eta_D$		40		%
3 dB Compression Point	$P_{-3dB}$	40			W

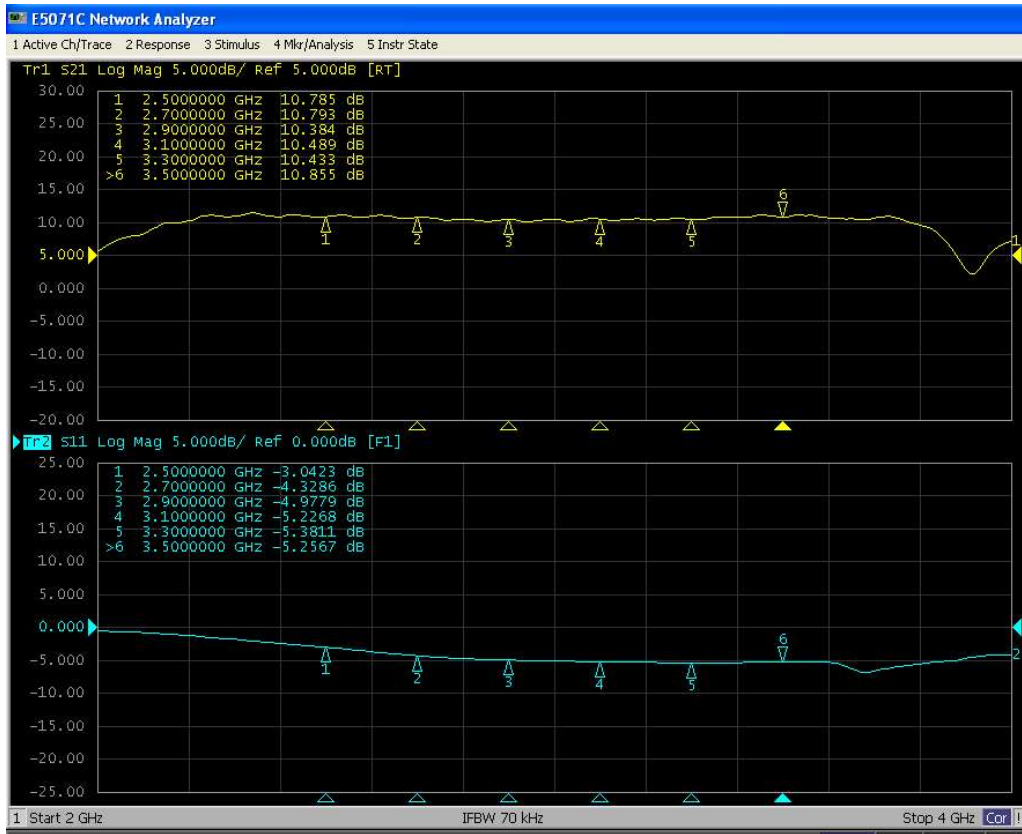
**Load Mismatch (In Innogration Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 50\text{mA}$ ,  $f = 2500\text{MHz}$

VSWR 5:1 at 40W pulse CW Output Power	No Device Degradation
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## 2.5-3.5GHz

### TYPICAL CHARACTERISTICS

Figure 2. Network analyzer output S11/S21 (VDS=28V IDQ=200mA VGS=2.95V)



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Figure 3. Test Circuit Component Layout

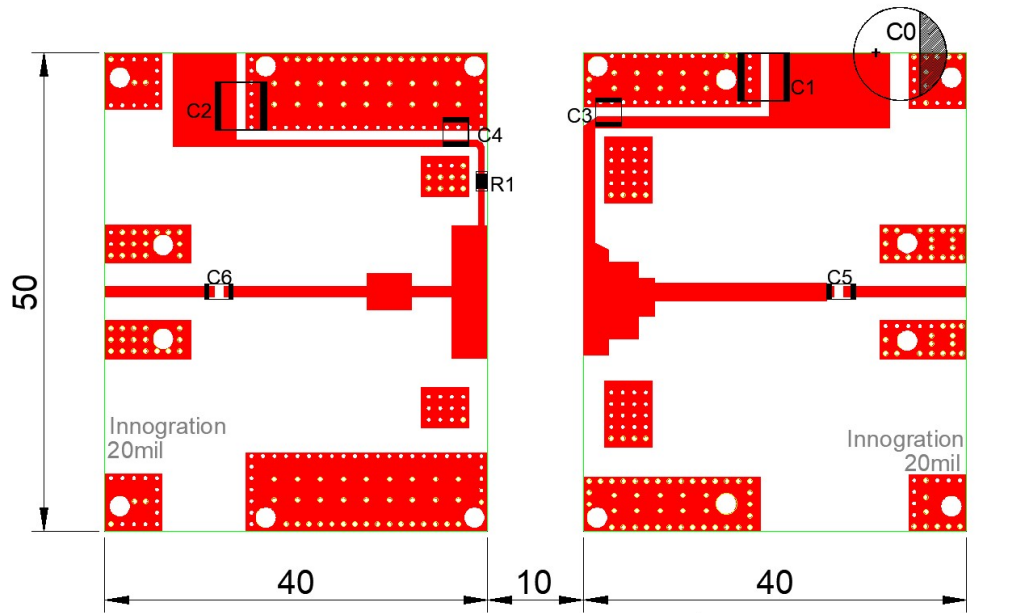


Table 5. Test Circuit Component Designations and Values

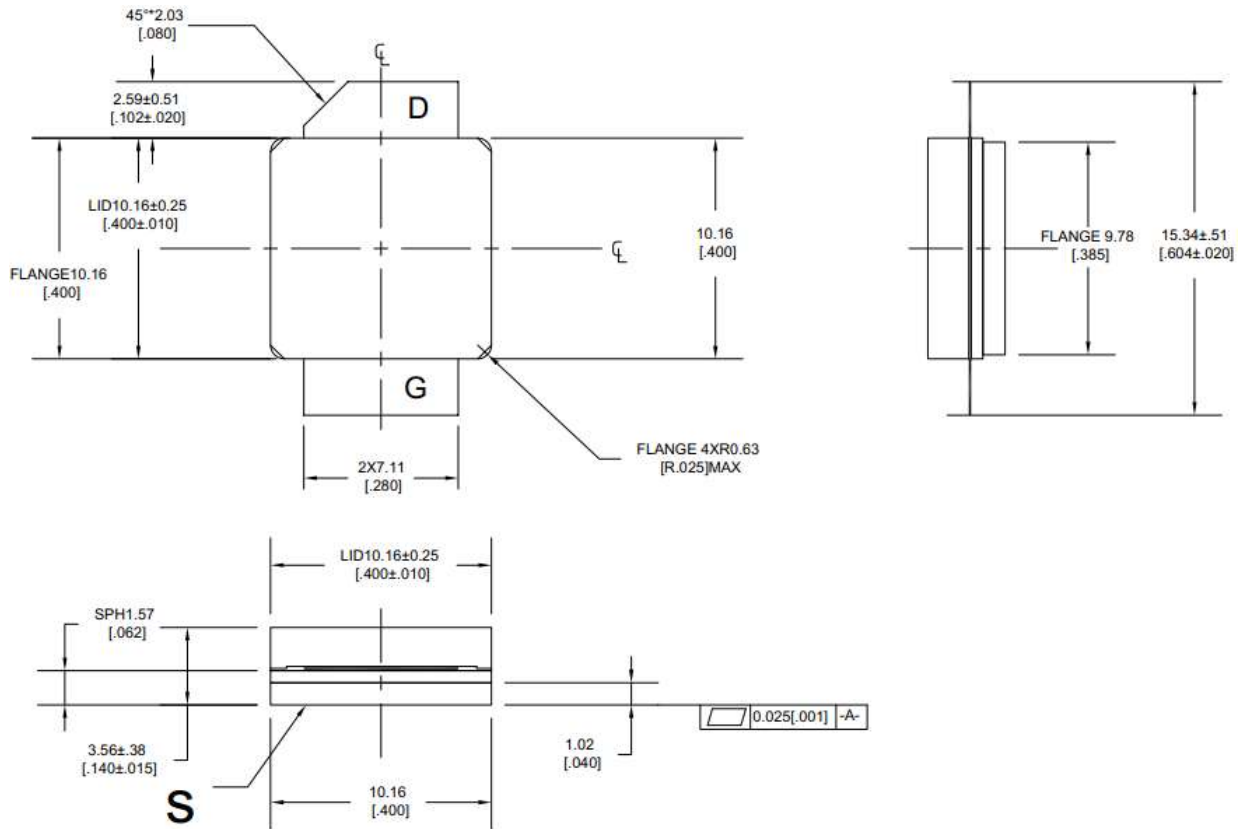
Component	Description	Suggestion
C0	470uF/63V	
C1,C2	10uF	5750
C3,C4,C5,C6	10pF	MQ301111
R1	Chip Resistor,10Ω	0805
PCB	20 Mil Rogers 4350B	

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## Package Outline

Earless flanged ceramic package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/24	Rev 1.0	Product Datasheet

Application data based on RXT-23-18

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