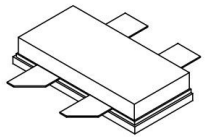
ITEV011K0B4 LDMOS TRANSISTOR

Document Number: ITEV011K0B4
Product Datasheet V1.0

1000W, 50V High Power RF LDMOS FETs

ITEV011K0B4



Description

The ITEV011K0B4 is a 1000-watt capable, high performance, unmatched LDMOS FET, designed for HF/VHF. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application.

- Typical Performance (On Innogration 130-160MHz wideband fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 200 mA, CW

Freq(MHz)	PsatW)	Gain(dB)	Eff(%)
130	900	18.3	77
145	1000	18	73
160	1070	17	71

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 1000W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.2	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.04	°C/W

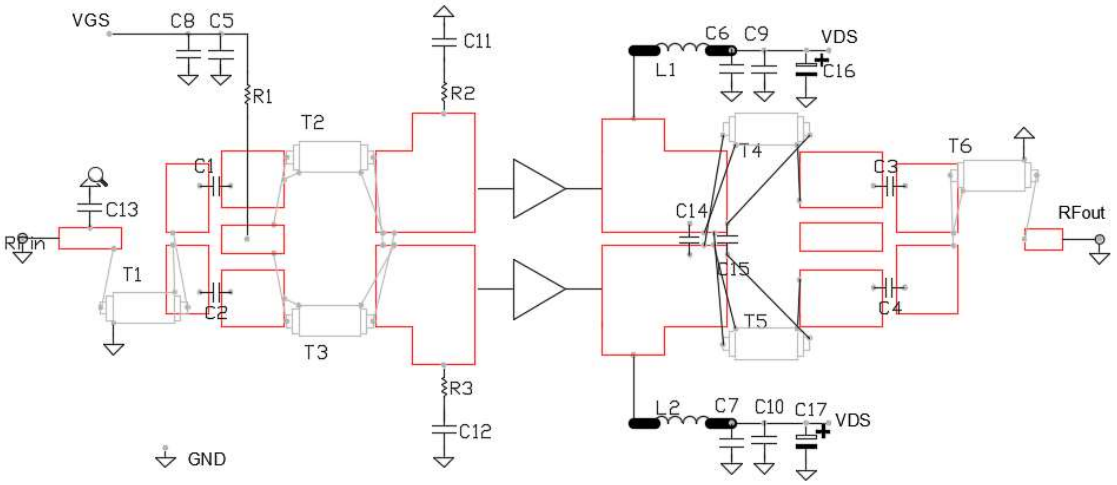
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (Per Side)					
Drain-Source Voltage V_{GS}=0, I_{DS}=18.0mA	$V_{(BR)DSS}$	130			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.14		V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		400		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		97		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.95		pF

Reference Circuit of Test Fixture (130-160MHz)



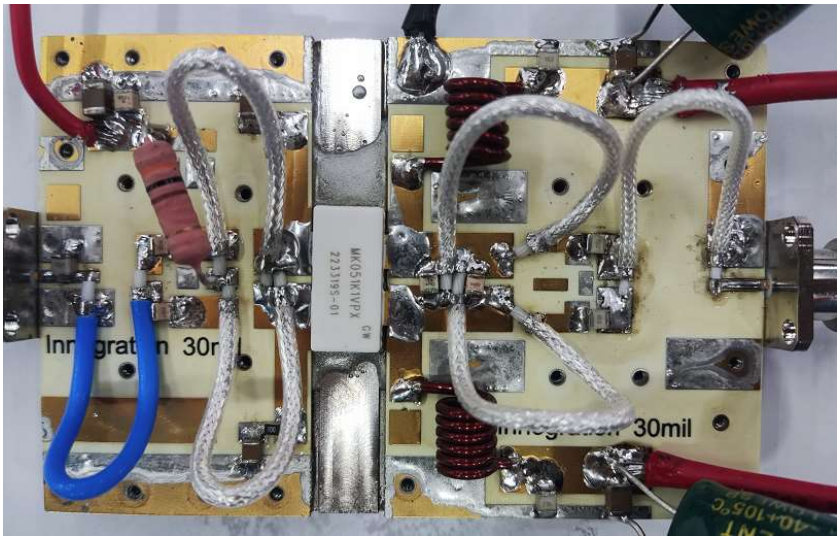
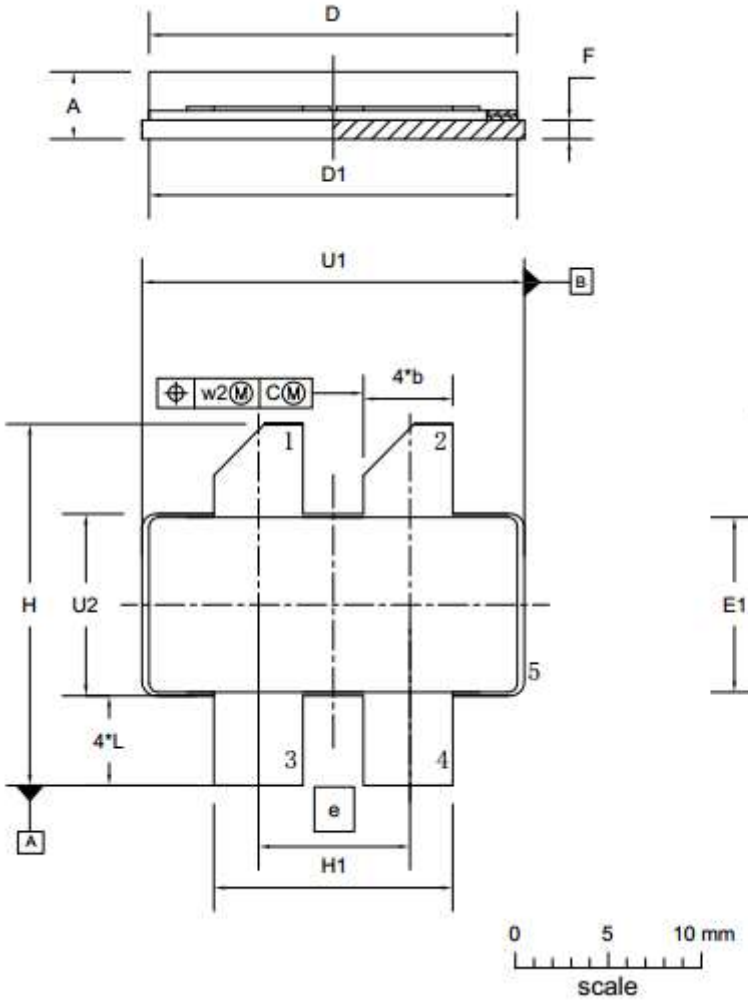


Figure 1. Test Circuit Component Layout for demonstration

Component	Description	Suggested Manufacturer
C1~C7	1000pF Beijing YN	MQ101111
C8~C10	Ceramic multilayer capacitor, 10uF, 100V	
C11,C12	Ceramic multilayer capacitor, 10uF, 50V	
C13	20pF Beijing YN	MQ101111
C14	47pF Beijing YN	MQ101111
C15	20pF Beijing YN	MQ101111
C16,C17	4700uF/63V Electrolytic capacitor	
R1	300Ω Plug-in electric resistance	
R2,R3	Chip Resistor,10Ω	
T1	50ohm 70mm	RFSFBU-086-50
T2,T3	12.5ohm 70mm 4:1	SFF-12.5-1.5
T4,T5	12.5ohm 70mm 9:1	SFF-12.5-1.5
T6	16.7ohm 70mm	SFF-16.7-1.5
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

Package Outline

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/9/1	Rev 1.0	Preliminary Datasheet
2023/2/28	Rev 1.0	Production Datasheet by renaming from MK011K1VPXS

Application data based on HL-22-37

Disclaimers